Service
Service
Service

MD 2.21 E
2.22 E
2.23 E
AA

Service Manual

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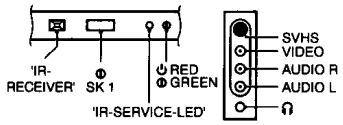
1. Technical specifications

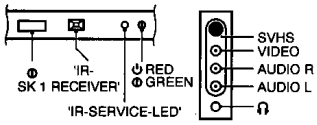
Mains voltage	: 220 - 240 V (± 10%)
	: 50 Hz - 60 Hz (± 5%)
Aerial input impedance	: 75 Ω - koaxial
Minimum aerial voltage	: 30 µV (VHF), 40 µV (UHF)
Maximum aerial voltage VHF/S/UHF	: 180 mV
Programmes	: 0 - 99
VCR programmes	: 0, 50 - 99

2. Connection facilities

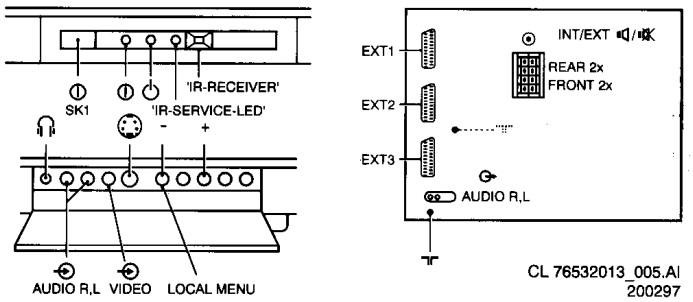
TOP CONTROL STYLING MIDDLE (FL6A)



TOP CONTROL STYLING RIGHT (FL6B)



TOP CONTROL STYLING (FL5)



Specification of the connectors

EXT 1 (AUX): RGB+CVBS

1	-	Audio ⊖ R (0.5V_{RMS} ≤ 1kΩ)
2	-	Audio ⊕ R (0.5V_{RMS} ≥ 10kΩ)
3	-	Audio ⊖ L (0.5V_{RMS} ≤ 1kΩ)
4	-	Audio ⊥
5	-	Blue ⊥
6	-	Audio ⊕ L (0.5V_{RMS} ≥ 10kΩ)
7	-	Blue (0.7V_{pp}/75Ω)
8	-	CVBS-status ⊕ 0-1.3V: INT 4.5-7V: EXT 16:9 9.5-12V: EXT 4:3
9	-	Green ⊥
10	-	-
11	-	Green (0.7V_{pp}/75Ω)
12	-	-
13	-	Red ⊥
14	-	RGB-status ⊥
15	-	Red (0.7V_{pp}/75Ω)
16	-	RGB-status (0-0.4V: INT) (1-3V: EXT/75Ω)
17	-	CVBS ⊥
18	-	CVBS ⊥
19	-	CVBS ⊖ (1V_{pp}/75Ω)
20	-	CVBS ⊕ (1V_{pp}/75Ω)
21	-	Earthscreen

EXT2 (VCR): SVHS+CVBS+RGB

1	-	Audio ⊖ R (0.5V_{RMS} ≤ 1kΩ)
2	-	Audio ⊕ R (0.5V_{RMS} ≥ 10kΩ)
3	-	Audio ⊖ L (0.5V_{RMS} ≤ 1kΩ)
4	-	Audio ⊥
5	-	Blue ⊥
6	-	Audio ⊕ L (0.5V_{RMS} ≥ 10kΩ)
7	-	Blue (0.7V_{pp}/75Ω)/C-out (project 50)
8	-	CVBS-status ⊕ 0-1.3V: int 4.5-7V: EXT 16:9 9.5-12V: EXT 4:3
9	-	Green ⊥
10	-	Control (project 50)
11	-	Green (0.7V_{pp}/75Ω)
12	-	-
13	-	Red ⊥
14	-	RGB-status ⊥
15	-	Red (0.7V_{pp}/75Ω), C-in/out
16	-	RGB-status (0-0.4V: INT) (1-3V: EXT/75Ω)
17	-	CVBS ⊥
18	-	CVBS ⊥
19	-	CVBS/Y ⊖ (1V_{pp}/75Ω)
20	-	CVBS/Y ⊕ (1V_{pp}/75Ω)
21	-	Earthscreen

EXT3: CVBS+audio

1	-	-
2	-	Audio ⊕ R (0.5V_{RMS} ≥ 10kΩ)
3	-	-
4	-	Audio ⊥
5	-	-
6	-	Audio ⊕ L (0.5V_{RMS} ≥ 10kΩ)
7	-	-
8	-	-
9	-	-
10	-	-
11	-	-
12	-	-
13	-	-
14	-	-
15	-	-
16	-	-
17	-	CVBS ⊥
18	-	CVBS ⊥
19	-	-
20	-	CVBS ⊕ (1V_{pp}/75Ω)
21	-	Earthscreen

Front

- ⊙ CINCH Video ⊕ 1V_{pp}/75Ω
- ⊙ CINCH Audio ⊕ L (2V_{RMS}; ≥ 10kΩ)
- ⊙ CINCH Audio ⊕ R (2V_{RMS}; ≥ 10kΩ)

⊙ 3.5mm / 🎧 32-2000Ω ≥ 10mW

SVHS

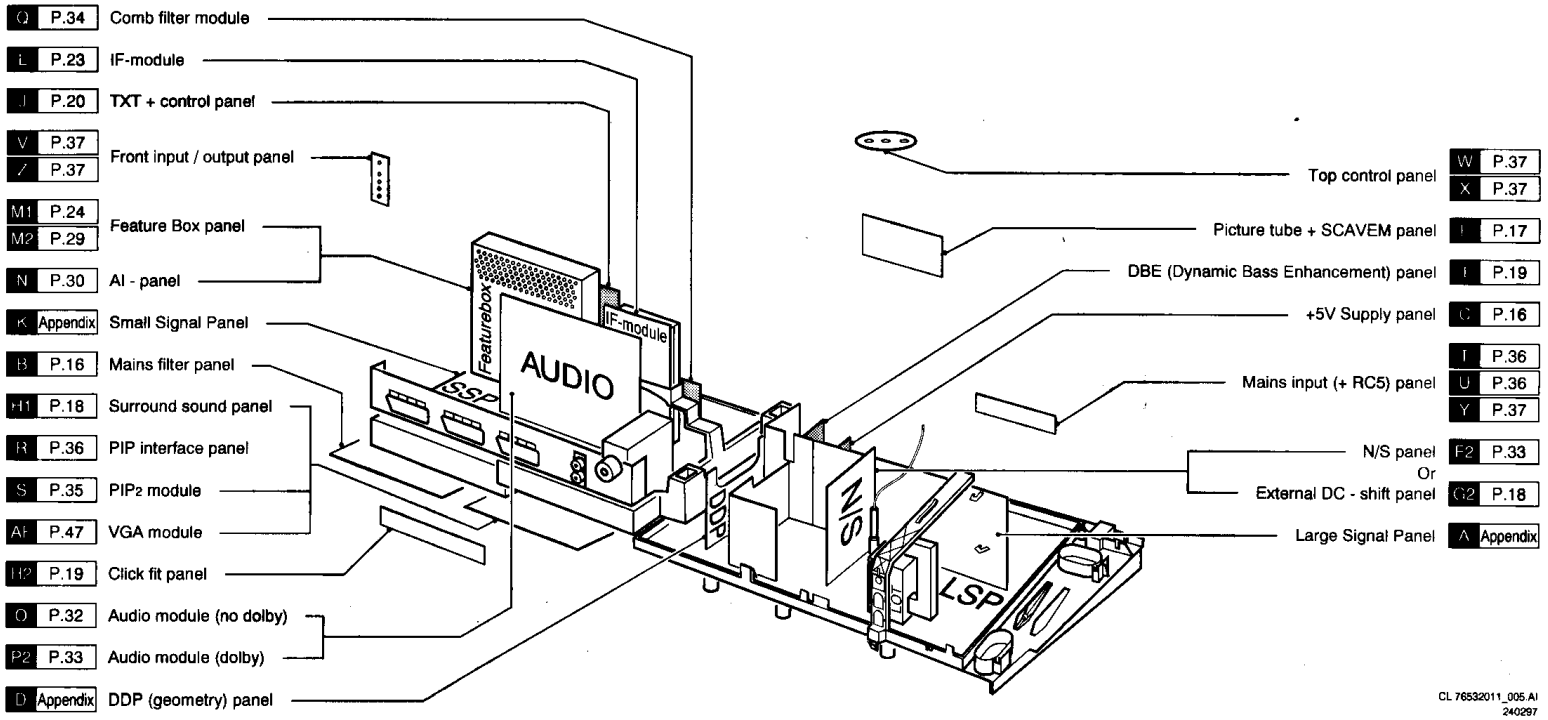
1	-	⊥
2	-	⊥
3	-	Y ⊕ (1V_{pp}; 75Ω)
4	-	C ⊕ (0.3V_{pp}; 75Ω)

Audio out (rear)

- ⊙ CINCH Audio ⊖ L (0.5V_{RMS}; ≤ 1kΩ)
- ⊙ CINCH Audio ⊖ R (0.5V_{RMS}; ≤ 1kΩ)

Chassis overview

Non Top Dolby version



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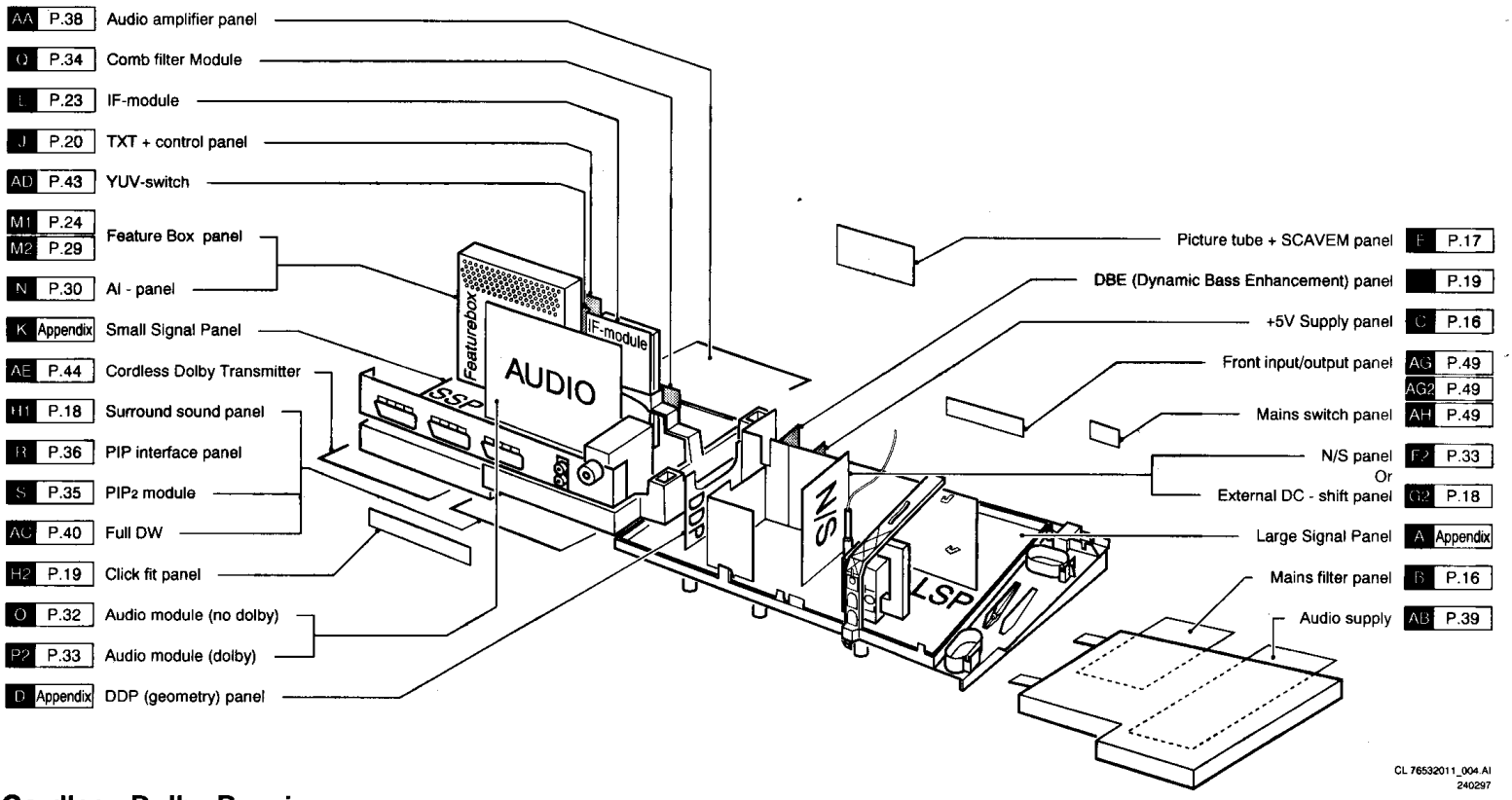
Top Dolby version



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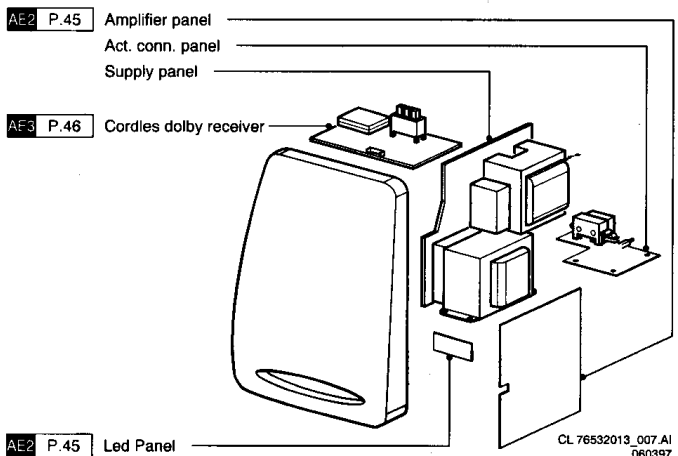
Cordless Dolby Receiver



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3. Safety instructions, Maintenance instructions,

Safety instructions for repairs

1. Safety regulations require that during a repair:
- the set should be connected to the mains via an isolating transformer
- safety components, indicated by the symbol ⚠ should be replaced by components identical to the original ones
- when replacing the CRT, safety goggles must be worn

2. Safety regulations require that after a repair the set must be returned in its original condition. In particular attention should be paid to the following points:
- As a strict precaution, we advise you to resolder the solder joints through which the horizontal deflection current is flowing, in particular:
  - ★ all pins of the line output transformer (LOT);
  - ★ fly-back capacitor(s);
  - ★ S-correction capacitor(s);
  - ★ line output transistor;
  - ★ pins of the connector with wires to the deflection coil;
  - ★ other components through which the deflection current flows.

Note:
This resoldering is advised to prevent bad connections due to metal fatigue in solder joints and is therefore only necessary for television sets older than 2 years.
- The wire trees and EHT cable should be routed correctly and fixed with the mounted cable clamps.
- The insulation of the mains lead should be checked for external damage.
- The mains lead strain relief should be checked for its function in order to avoid touching the CRT, hot components or heat sinks.
- The electrical DC resistance between the mains plug and the secondary side should be checked (only for sets which have a mains isolated power supply). This check can be done as follows:
  - ★ unplug the mains cord and connect a wire between the two pins of the mains plug;
  - ★ set the mains switch to the on position (keep the mains cord unplugged!);
  - ★ measure the resistance value between the pins of the mains plug and the metal shielding of the tuner or the aerial connection on the set. The reading should be between 4.5 MΩ and 12 MΩ;
  - ★ switch off the TV and remove the wire between the two pins of the mains plug.
- The cabinet should be checked for defects to avoid touching of any inner parts by the customer.

Maintenance instruction

It is recommended to have a maintenance inspection carried out by a qualified service employee. The interval depends on the usage conditions:
- ★ when the set is used under normal circumstances, for example in a living room, the recommended interval is 3 to 5 years;
- ★ when the set is used in circumstances with higher dust, grease or moisture levels, for example in a kitchen, the recommended interval is 1 year.

The maintenance inspection contains the following actions:
- ★ execute the above mentioned 'general repair instruction';
- ★ clean the power supply and deflection circuitry on the chassis;
- ★ clean the picture tube panel and the neck of the picture tube.

Warnings

1. In order to prevent damage to ICs and transistors, all high-voltage flashovers must be avoided. In order to prevent damage to the picture tube, the method shown in Fig. 3.1 should be used to discharge the picture tube. Use a high-voltage probe and a multimeter (position DC-V). Discharge until the meter reading is 0V (after approx. 30s).

2. **ESD**

All ICs and many other semiconductors are sensitive to electrostatic discharges (ESD). Careless handling during repair can drastically shorten the life. Make sure that during repair you are connected by a pulse band with resistance to the same potential as the earth ot the unit. Keep components and tools also at this same potential.

3. Together with the deflection unit and any multipole unit, the flat square picture tubes used form an integrated unit. The deflection and the multipole units are set optimally at the factory. Adjustment of this unit during repair is therefore not recommended.

4. Be careful when taking measurements in the high-voltage section and on the picture tube.

5. Never replace modules or other components while the unit is switched on.

6. When making settings, use plastic rather than metal tools. This will prevent any short circuits and the danger of a circuit becoming unstable.

7. On this unit the 141 volt supply voltage is not supplied via an interconnection on the deflection yoke to the line output transformer. Whenthe deflection cable is detached, the + 141 volt supply remeins loaded. In orderto unload the + 141 volts, coil 5136 should be removed.

Warnings and Notes

Notes

1. The direct voltages and oscillograms should be measured with regard to the tuner earth (⊥), or hot earth (⏚) as this is called.

2. The direct voltages and oscillograms shown in the diagrams should be measured in the **Service Default Mode** (see chapter 6) with a colour bar signal and stereo sound (L: 3 kHz, R: 1 kHz unless stated otherwise) and picture carrier at 475.25 MHz.

3. Where necessary, the oscillograms and direct voltages are measured with (⊤) and without aerial signal (⊁). Voltages in the power supply section are measured both for normal operation (⏻) and in standby (⏻). These values are indicated by means of the appropriate symbols.

4. The picture tube PWB has printed spark gaps. Each spark gap is connected between an electrode of the picture tube and the Aquadag coating.

5. The semiconductors indicated in the circuit diagram and in the parts lists are completely interchangeable per position with the semiconductors in the unit, irrespective of the type indication on these semiconductors.

6. DOLBY SURROUND PRO • LOGIC

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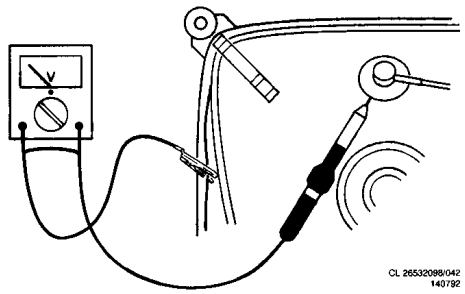


Fig. 3.1

4. Mechanical instructions

The MD2 chassis has predefined service positions for different panels. To get access to the chassis, first do the following steps:

1. Unscrew the 4 screws fixing the rear cover to the rear cover plate (cover plate with the scart plugs).
2. Unclick the 4 clicks at the top side and upper left and right side by pushing (no torquing is required) the clicks while pushing the rear cover a little.
3. Unscrew the remaining 4 screws.
4. Take of the rear cover.

Service position LSP component side

1. Remove the subwoofer by disconnecting the cable and lift it.
2. Put the SSP in the horizontal service position (see horizontal service position SSP) or the 30 degree position.
3. Remove the screw (1) in the bracket of the LOT. Remove this bracket by pushing the click (2) en pull it upwards.
4. Release clicks (3) and (4).
5. Lift the LSP PWB out of its bracket and pull it a little back.

PS: After taking out the mains cord from its fixation clicks, the entire bottom plate with the chassis in it can be released from the cabinet and then shifted back to create more space.

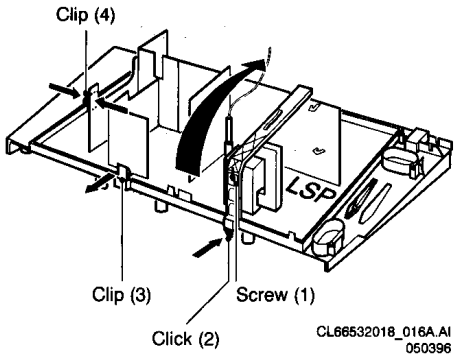


Fig. 4.1

Service position LSP copper side

Two possibilities:

With a table:

1. Bring the LSP in the service position component side (see above).
2. Take all wiring out of the fixation brackets (on the rear side of the chassis and under the picture tube).
3. Dismount the mains input panel from the SSP bracket and lay it on the table (this gives more freedom of the mains cable N01-L01).
4. Disconnect the degaussing coil (connector L02).
5. Disconnect the rotation coil (connector Y90) if fitted.
6. Carefully pull back the LSP and put it on its front side.

Without a table by making use of cable extension kit 4822 310 10674:

1. Disconnect all cables at the LSP side.
2. By now the LSP can be turned to a vertical position (5), copper side at the right hand with the LOT above. For this vertical position special slides are made in the bottom plate of the cabinet.
3. The LSP can be fixed to the bottom plate by using the special pin marked M2. This pin is part of the bottom plate and must be broken out and placed into the hole (6) in the bottom plate.
4. Now reconnect L11-S11, L15-S15, L10-S10 and L01-N01 by **replacing** the cables by the cables of the cable extension kit 4822 310 10674.
5. By now the video processing is totally reconnected.
6. In case audio reproduction is required:
   For non-dolby sets:
   * Reconnect the Audio Module to the audio amplifier on the LSP (I28-L28).
   * Disconnect the plug at the left speaker side (seen from the rear).
   * Reconnect the green connector L38 (now the right speaker (seen from the rear) is connected).

   For dolby sets the centre speaker can be used or the Left and Right speaker by connecting this cable to V32 on the Surround Sound panel.

Remark: Leave the special pin in the special hole on the bottom plate of the set after the repair.

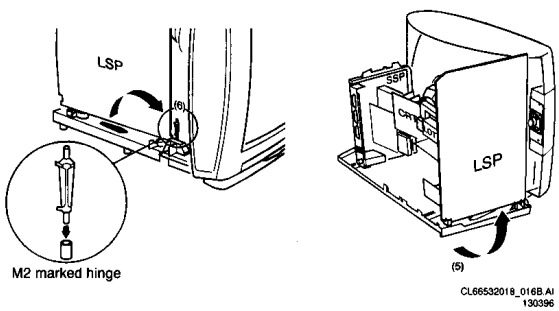


Fig. 4.2

Vertical service position SSP (solder side)

1. To reach for the SSP first the plastic rear cover plate (7) must be removed by putting a screwdriver in the hole (8) and move it upwards. Now the rear cover plate can be removed by lifting it in the direction of the arrow.

2. To have access to the copper side of the SSP, the brackets clicked on the left side (seen from the back) from the SSP bracket must be removed:
   * Upper bracket; Pushing the click (9) away and slide the bracket according the arrow upwards.
   * Lower bracket; First dismount the upper bracket, then push click (10) away and pulling it upwards according the arrow.

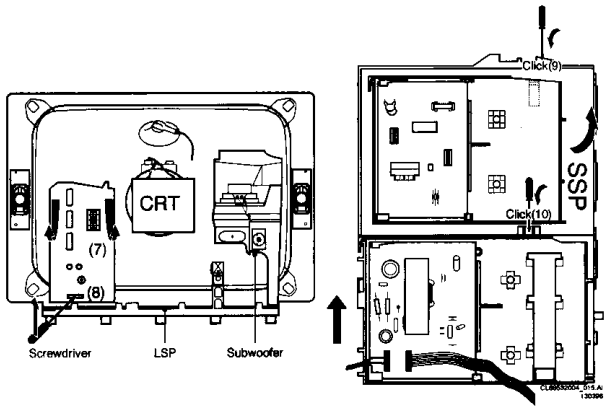


Fig. 4.3

Horizontal service position SSP (component side)

1. Push down the clicks of the SSP bracket (11) and simultaneously shift the complete SSP bracket including panels to the left (seen from the rear).

2. Take the SSP bracket (including all panels) out of the bottom plate and shift it a little to the right (seen from the side).

3. Put the SSP-bracket in the special holes on the bottom plate.

4. Now the SSP component side and all the panels mounted on the SSP are accessible.

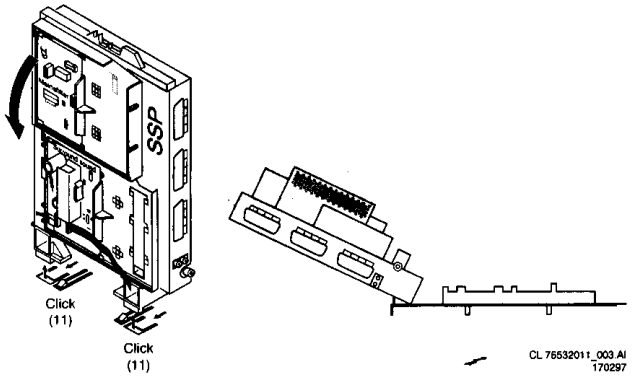


Fig. 4.4

Extra service position SSP for front operation (FL5)

1. Push the clicks of the SSP bracket down and at the same time slide the entire SSP bracket, including the panels, to the left (viewed from the rear)

2. Where necessary remove the wiring from its clicks

3. Tilt the SSP bracket (with all panels) into its 30 degree position

This 'extra' service position for the SSP bracket can be used in all MD2.2 sets.

Service position Feature Box by using cable extension kit 4822 310 10674

With the use of the same extension kit as used for the vertical LSP service position, the Feature Box can be placed away from the SSP.

1. Put the SSP in the horizontal service position.

2. Remove the fixation bracket which holds the feature box and the IF-module by unscrewing the 2 screws (12) and then take out the fixation bracket. Take care for the 2 clicks of this bracket clicked in the feature Box shielding.

3. Click out the Feature Box and connect it to the SSP making use of the cable extension kit 4822 310 10674.

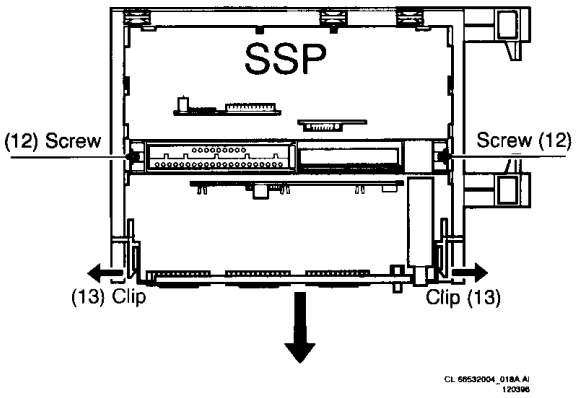


Fig. 4.5

Service position SSP PWB

First remove all cables where needed. Then remove the screws (12) in the bracket. The SSP PWB can be removed after loosing the two clicks (13), then slided backwards (in the direction of the arrow on the SSP bracket) and then taken out of the bracket.

Mechanical instructions

Removing the small panels out of brackets clicked on the SSP bracket

To dismount the panels itself which are mounted in the brackets clicked on the SSP bracket, the following has to be done:

- Upper panel; Open click 14 and 15 and take out the panel mounted in the upper bracket. Lay the panel on a table.
- Lower panel; Open click 16 and 17 and take out the panel mounted in the lower bracket. Lay the panel on a table.

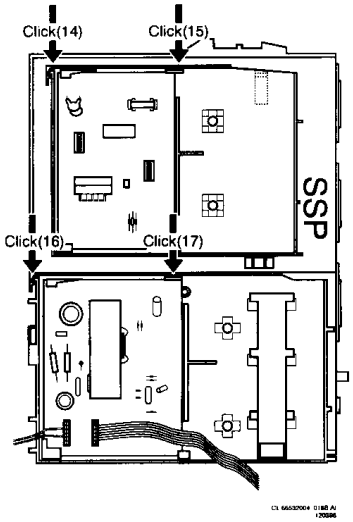


Fig. 4.6

Two possibilities:

Service position bracket including panels:

1. Remove the fixing bracket by means of its clicks.
2. Remove the subwoofer so that a place is created to be able to remove the module directly.
3. Push both clicks (18 + 19), which secure the large bracket to the bottom plate, upwards at the same time.
4. Pull the entire module to the back while the clicks are being held up.
5. Remove the entire bracket, including the modules, from the bottom plate.
6. Lay the entire module with the modules, pointing upwards, on the bottom plate.

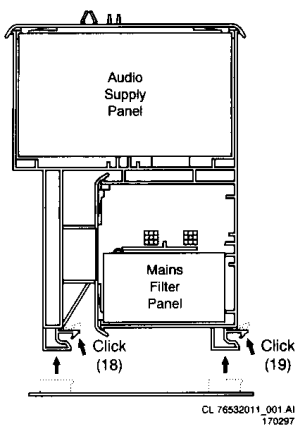


Fig. 4.7

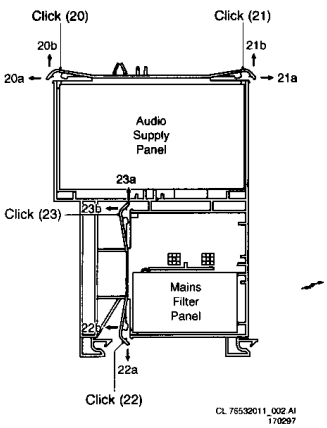


Fig. 4.8

Service position of the 'Audio Power Supply' or the 'Mains Filter' itself:

1. Leave the large bracket in its vertical position, but remove the fixing bracket between the large bracket and the subwoofer.
2. Click the large clicks on the large bracket free.
   * For the 'Audio Power Supply' the two large clicks (20 + 21) on the top.
   * For the 'Mains Filter' the large click on the bottom left (22) and then the small click halfway on the left (23).
3. Remove the wiring from its clamps.
4. The module can now be removed from the bracket and placed on a table.
5. During assembly make sure that the module is re-clamped correctly BEHIND its grip.

Service position VGA interface panel in the 28"

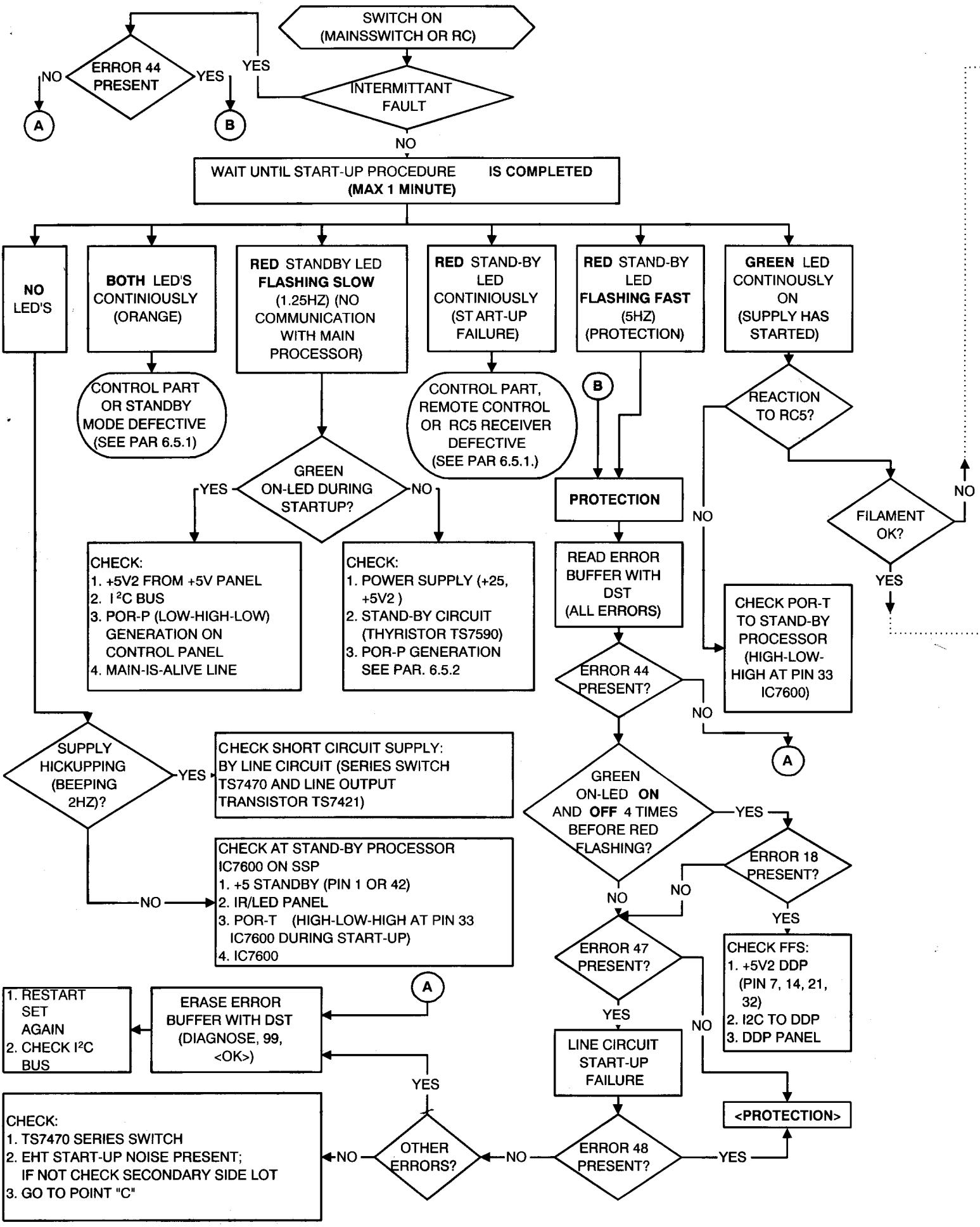
1. Carefully remove the entire bottom plate including LSP and SSP from the cabinet and place it a few centimetres to the rear (watch out for the picture tube panel).
2. Pull the wiring loose to the front.
3. Click the VGA interface panel free.

Service position front operation

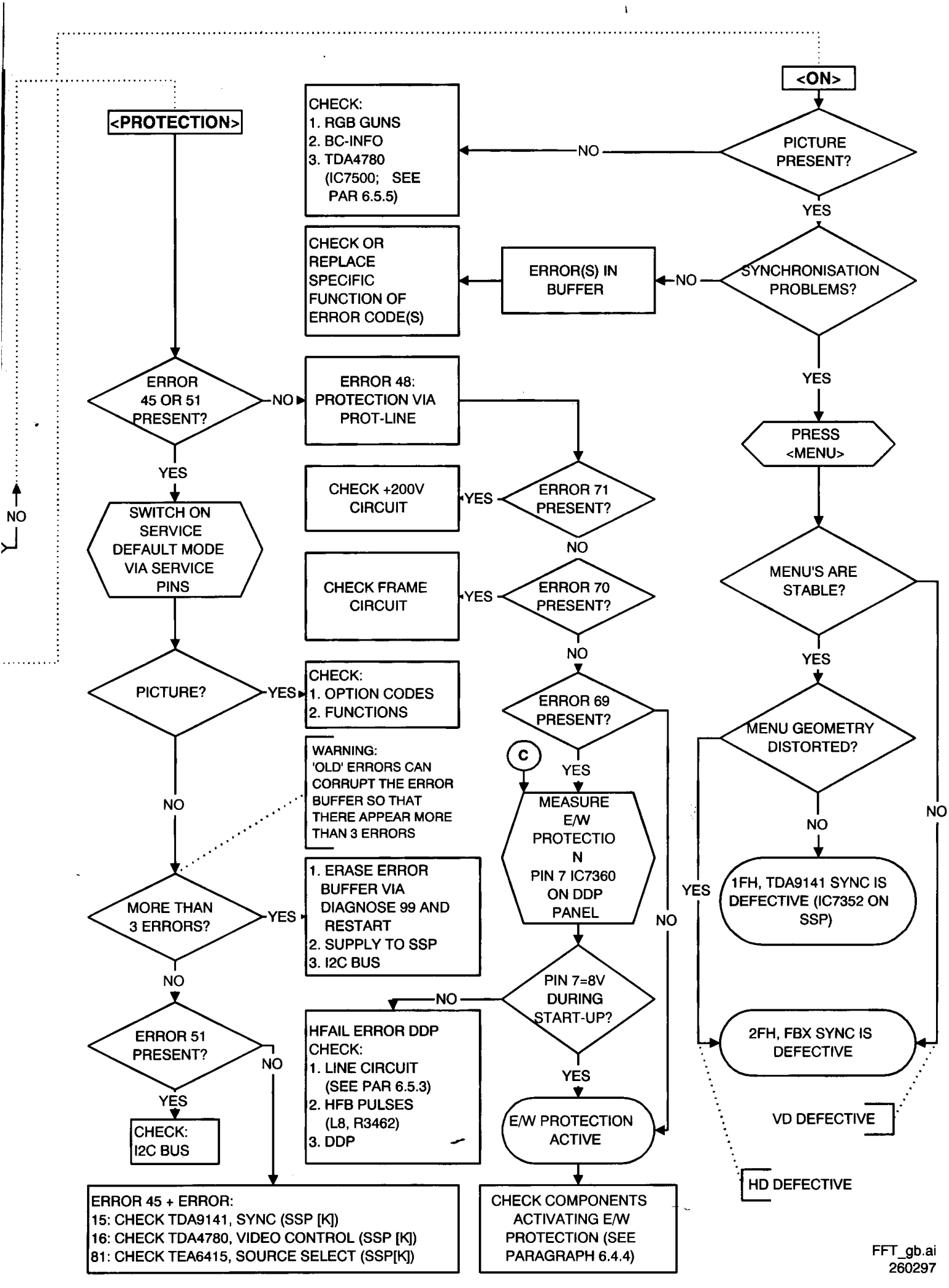
In sets with front operation (FL5 styling), knobs and LED's are located under the picture tube. All front panels and centre loudspeakers are mounted in a plastic bracket which can be removed in its entirety.

1. In order to be able to remove the bracket, the screws between the picture tube and the bottom plate on the inside of the cabinet are to be removed together with the screws which are located on the bottom of the cabinet. In order to be able to remove these screws easily the set will have to be turned. It is preferred that the set is turned with the back cover fitted.Turn the set so that the picture tube is pointing down and place the set carefully onto a soft and clean surface.
2. After the screws have been removed the set can be brought back to the normal position.
3. After removing the screws on the inside, the bracket can be removed via the bottom.

6. Service modes, DST, Error messages, Protections, Fa



Faultfinding and Repair tips



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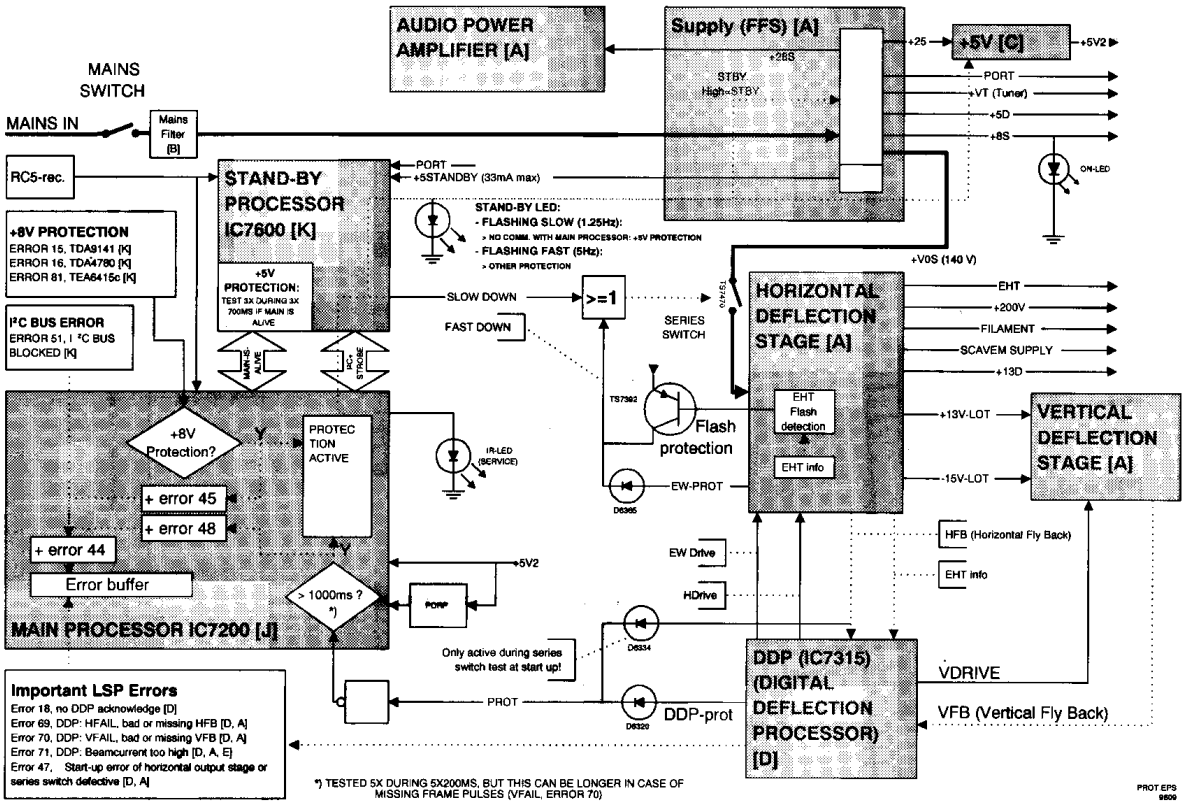
Protection diagram

MD 2.21/2.22/2.23 E protection diagram (2fH versions)



Error code table

Error	Device	Description	Item	Panel	Defective module indication in SAM	MD2.1	MD2.2
0	no error		-	-	No errors	x	x
4	ST24C16B1	NVM EAROM 2048 bytes	7201	SSP	Control	K	K
6	UV916S	Tuner	1100	SSP	Tuner	K	K
15	TDA914X	Video + sync processor	7352	SSP	Video processing (SSP)	K	K
16	TDA4780	Video controller	7500	SSP	Video control	K	K
18	TDA9155	DDP processor	7315	DDP (Geometry)	Geomtry processor	D	D
28	SAA5270	TXT processor	7400	TXT	Teletext	J	J
29	PCF83CE652_ featurebox	FBX microprocessor	7505	FBX	Feature box	M	M
33	SDA9288_2_pip2	PIP-processor	7788	PIP	PIP	S	S
34	UV12xx	PIP or DW tuner	1775 / E9F1	PIP / DW	PIP / Video DualScreen	S	S / AC
36	PCF8574_pip	I/O-expander for PIP forced colour	7860	PIP	PIP	S	S
37	SAB9077H_dwi	PIPO (Picture In Picture Out)	IC9A	Video DualScreen	Video DualScreen	-	AC
38	PCF8574_dwi	I/O-expander for DW	IC9N	Video DualScreen	Video DualScreen	-	AC
39	TDA914x_dwi	Video + Sync processor for DW	IC9J	Video DualScreen	Video DualScreen	-	AC
44	SW_protection (uP has decided for protection)	Generated after error code 51, 18, 69, 70 or 71	-	-	SW Protection	x	x
45	Supply_8V	TDA4780 + TDA914x + TEA6415 (+ TDA9860)	-	-	+8V Supply error	K	K
47	+140Vserie_switch_ protection	Series switch protection (only checked at start up)	-	LSP	Series switch 140V	A	A
48	Protection (prot-line)	Hardware protection (activated by the PROT-line)	-	LSP + DDP	HW protection	A+D	A+D
51	I2c_slow_bus	Blocked I2c slow-bus (shorted SDA, SCL or SDA to SCL)	-	-	I2C bus blocked	x	x
58	TDA9860_vds	Sound processor on Dolby Audio Module for Video DualScreen	7590	Dolby Audio Module	Audio module	-	P
64	TDA9177_LTP	Line Transient Processor	7580	SSP	Video control / picture signal imrpov.	-	K
69	Protection_hfail	Horizontal deflection error (DDP protection)	-	DDP + LSP	Horizontal circuit	D	D
70	Protection_vfail	Vertical deflection error (DDP protection)	-	DDP + LSP	Vertical circuit	D	D
71	Protection_overcurrent	Overcurrent protection (DDP protection); beam current too high	-	DDP + LSP	Beam current	D	D
79	TDA9860_DW	Sound processor for DW	-	-	-	-	AC
80	MSP3400/3410	FM/NICAM decoder and audio source select	7353	Audio module	Audio module	O/P	O/P
81	TEA6415	Source select video matrix	7406	SSP	Source select	K	K
82	TMP47C640/840	Standby(I/O)-processor	7600	SSP	Standby processor	K	K
85	SAA7710T	Dolby processor	7600	Dolby audio	Audio module	O/P	O/P
86	PCF8574A	I/O-expander for frame rotation	7050	N/S + ROT	Rotation panel	F2	F2
88	TSA5520	Wireless dolby	1403	Wireless dolby trans	Dolbt transmitter	-	AE1

In this chapter the following paragraphs are included:

6.1 Test points
6.2 Service modes and Dealer Service Tool
6.3 Error codes
6.4 Protections
6.5 Faultfinding and repair tips

6.1 Test points

The MD2 chassis is equipped with test points in the service printing. These test points are referring to the functional blocks:

* P1-P2-P3, etc: Test points for the power supply
* L1-L2-L3, etc: Test points for the line drive and line output circuitry
* F1-F2-F3, etc: Test points for the frame drive and frame output circuitry
* S1-S2-S3, etc: Test points for the synchronisation circuitry
* V1-V2-V3, etc: Test points for the video processing circuitry
* I1-I2-I3, etc: Test points for the IF part
* A1-A2-A3, etc: Test points for the audio processing circuitry
* C1-C2-C3, etc: Test points for the control circuitry
* T1-T2-T3, etc: Test points for the teletext processing circuitry

The numbering is done in a for diagnostics logical sequence; always start diagnosing within a functional block in the sequence of the relevant test points for that functional block.

6.2 Service modes and Dealer Service Tool (DST)

Together with the GFL chassis a dealer remote control is introduced, the RC7150 which is called the Dealer Service Tool or DST. This RC7150 is a remote control for the dealer and the servicer and is fully compatible with the MD2.

6.2.1 Installation features for the dealer

The dealer can use this remote control for programming the TV-set with presets, TV-settings, Dish settings and Logo's. Just like the GFL, the MD2 and a lot of existing sets like MD1, AA5, FL, GR2, G90B, G110 and the new Philips VCR series using the so called NORA deck can be programmed with it.

One of the innovative features of the Dealer Service Tool is the way in which it is programmed. A complete list of presets can simply be downloaded from the MD2 (and GFL) into the Dealer Service Tool.
To make this download possible, a two way communication link, the so called 'dealer link', is set up between the RC7150 and the MD2 TV-set. To establish this link, the MD2 sets are equipped with an additional Infra Red transmitter LED and the RC7150 has an Infra Red receiver on board. The Dealer Link however only works on short distance, up to 10 cm or 4 inches.
For explanation of the installation features of the DST, the directions for use of the DST are recommended (use code 4 for correct downloading).

The figures below show the position of the DST for the different types of styling:

Styling with top centre operation:

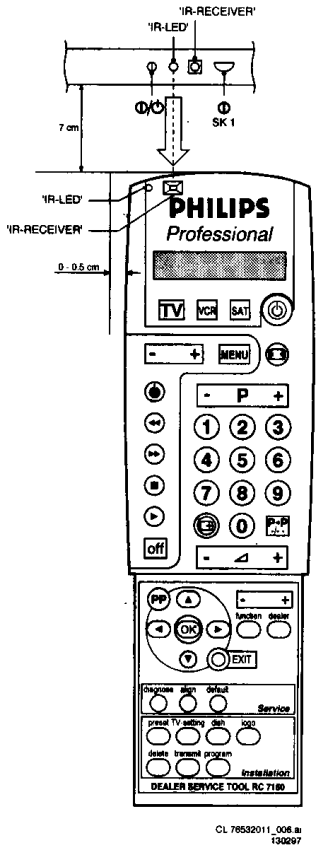


Fig. 6.1

Styling with top right operation:

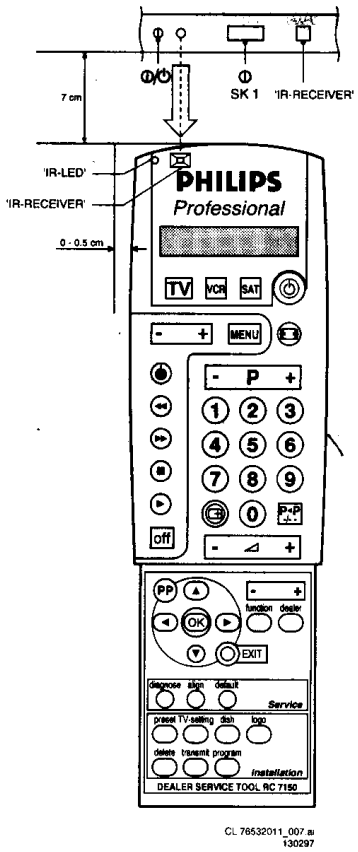


Fig. 6.2

Protections, Faultfinding and Repair tips

Styling with front operation:

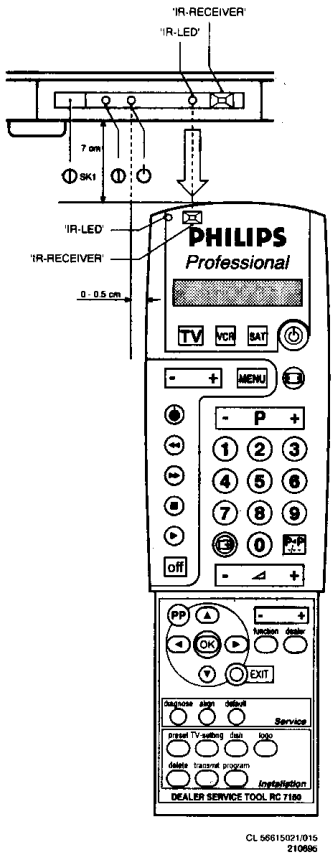


Fig. 6.3

Dealer Mode
Press the 'DEALER' key on the DST to enter the Dealer Mode. In the dealer mode some settings can be changed in order to customize the set.

6.2.2 Diagnose features for the servicer

The MD2 sets can be put in the various service modes via the DST RC7150. The Service Alignment Mode and the Service Default Mode can also be entered by connecting the pins on the SSP.

Service Default Mode (SDM)
Specification of the SDM:
- Tuning frequency 475.25 MHz;
- TV-system for BGLM set to BG, for BGLL'I sets to LL';
- All picture settings at 50% (brightness, colour, contrast, HUE);
- All sound settings at 50% except volume at 25% (so bass, treble, balance at 50%, volume at 25%);
- All service-unfriendly modes are disabled (like sleep timer, child lock, automatic switch off, blue mute).

Entering the SDM can be done in 2 ways:
- By the 'DEFAULT' key on the DST while the set is in the normal operation mode.
- By shortcircuiting the two pins on the component side of the SSP with the indication 'SERVICE DEFAULT MODE' (activation can be performed in all modes except when the set has a problem with the main-processor (indicated by a slow (1.25Hz) blanking LED)).

Note: If the SDM is entered via the pins, the Series Switch protection (error 47) and the +8V protection (error 45) is de-activated.

Exiting the SDM can only be done via the STANDBY command. By switching off-on the set with the mains switch the MD2 will come up again in the SDM.

Service Alignment Mode (SAM)
Specification of the SAM:
- Software alignments (see chapter 8);
- Option settings (see chapter 8);
- Error buffer reading and erasing. The most recent error code is displayed on the left side;
- Operation counter;
- Software version.

Entering the SAM can be done in 2 ways:
- By the 'ALIGN' key on the DST while the set is in the normal operation mode (or SDM). Enter the password '3-1-4-0' and press OK.
- By shortcircuiting the two pins on the component side of the SSP with the indication 'SERVICE ALIGNMENT MODE' (activation can be performed in all modes except when the set has a problem with the main-processor (indicated by a slow (1.25Hz) blanking LED)).

  Note: If the SAM is entered via the pins, the Series Switch protection (error 47) and the +8V protection (error 45) is de-activated.

Exiting the SAM can be done via the MENU command or via switching off-on the set with the mains switch.

Customer Service Mode (CSM)
In order to be able to deal with 'house repairs' and ' nuisance calls' better in the future, the so-called 'Customer Service Mode' will introduced in all future chassis relevant for this. This 'Customer Service Mode' (CSM) is a special service mode which can be activated and deactivated by the customer. This CSM is a 'read only' mode, therefore the customer is unable to write into this.

The customer activates the CSM by pressing and holding the 'MUTE' button on the remote control for at least 4 seconds at the same time as pressing the MENU button on the TV. This activation only works if there is no menu on the screen.

The customer deactivates the CSM by:
- selecting any button on the remote control;
- switching the set off (mains switch) and then switching back on again.

The following settings are displayed in the CSM:
- Software version.
- Error code buffer.
- Overall setting of the PP (Personal Preference) values for volume, colour, brightness, contrast (all 0-63) and focus (0-4).
- Dolby Signalling detection indication: 'Present' or 'Not Present'.
- Attention: the presence of Dolby can only be tested by the software on the Dolby Signalling Bit. If a Dolby transmission is therefore received without a Dolby Signalling Bit, then this indicator will show 'not present' even though such a Dolby transmission is received.

- Overall setting of the Surround Mode: 'Pro Logic' or 'Dolby 3 Stereo' or 'Hall' or 'Off'.
- Overall setting of the Rear Volume (0-63); volume of the surround sound speakers in 'Pro Logic' or 'Dolby 3 Stereo' or 'Hall' mode.
- Overall setting of the Centre Volume (0-63); volume of the centre speakers in 'Pro Logic' or 'Dolby 3 Stereo' mode.
- Local setting of the DNR and a value for the noise number (good signal 0-2, average signal 4-5, bad signal 7 or higher).
- Overall setting of the Digital Option ('100 Hz', 'Digital Scan' or 'Natural motion').
- Local setting / detection of TV and Audio system information: 'NICAM'/'MONO'/'A2' (analogue stereo sound) /'DUAL' and 'PAL'/'SECAM'/'NTSC'.
- Detuned bit is 'Yes' or 'No';
  This bit indicates whether the selected programme is stored after a micro-search or not: for 'Yes' the programme is stored via manual entry of the frequency when a transmitter was not present on that frequency. In that case the TV will attempt to perform a micro-search every time the programme number is selected. Once the micro-search has been successful the Detuned Bit will be set to 'No'.
- Overall setting of the configuration menu for 'VCR type' is 'PALplus' or 'Non PALplus';
  If PALplus VCR type is selected the luminance and chrominance on the PALplus panel is decoded for the VCR signal. If this configuration is set incorrectly this will result is stripes on the picture.
- Overall setting in the configuration menu for 'CD-i/Photo-CD' is 'Present' or 'Not Present';
  If 'Present' is selected the starting point is a top quality signal and a number of settings are therefore changed automatically. If this configuration is set incorrectly this will result in a worse picture quality.

All settings are displayed in 'real time'. The settings displayed are therefore the settings which were set at the moment of activating the CSM. The 'overall' settings apply for all programmes, the 'local' settings are only for that programme viewed that was selected at the moment at which the CSM was activated.

The screen appears as follows:

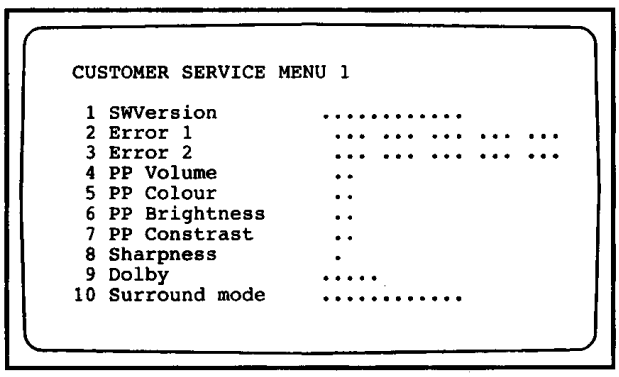


Fig. 6.4a

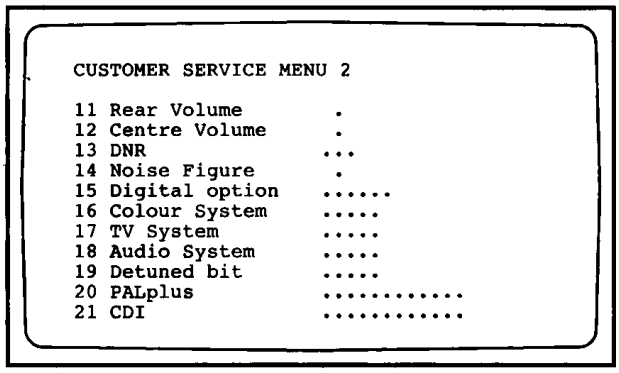


Fig. 6.4b

Diagnose Mode (only active during transmission of error codes and diagnose 99)
This mode is activated by the DIAGNOSE command on the DST for reading the error codes and erasing the error buffer by the DST even when the set is in protection and so there is no picture (assuming that the power supply and the control part are working). For activation see paragraph 6.3. The diagnose Mode is only a temporarily mode (the set will go back to the previous mode), and can not be switched on permanently.

Note: The diagnose mode can not be entered if the SAM is activated.

6.3 Error codes

6.3.1 Reading error codes from the error buffer

The error buffer can be read in 2 ways:

1. On the screen via the Service Alignment Mode (SAM):
   In case picture is OK, the error buffer can be read the easiest via the SAM. In the main menu of the SAM the last 10 different error codes occurred are displayed. The most recent detected error code is displayed on the left side, so e.g.:
   - 0 0 0 0 0 means no error codes present in the buffer
   - 3 0 0 0 0 means one error code present in the buffer; error code 3
   - 2 3 0 0 0 means two error codes present in the buffer; error code 2 is the most recent, error code 3 is detected before 2.

2. On the display of the DST:
   If an error has been detected by the MD2 chassis, the set might go into protection. Without the presence of a picture the errors can be read by the DST, as long as the main-processor is still active (green LED continuous and red LED blinking fast (5Hz); in case of red LED is blinking slow (1,25Hz) there is a main-processor problem).

To transmit the errors from the TV to the DST:
1. Press the 'DIAGNOSE' key (in all modes except the SAM);
2. Press '1' to view the last error detected;
3. Hold the DST 5 to 10 cm from in front of the stand-by LED of the set (the IR-sending LED of MD2 is located near the stand-by LED);
4. Press the 'OK' key.

The error is represented by a 2 digit number.
The 2 digits on the DST are displayed sequentially, with a pause before it is repeated. The digit after the pause is the 1st digit.
If the display reads 4 - 7, the error code is 47. To read other error codes, press 'DIAGNOSE' and one of the other digit keys.

Note:
- If the DST cannot communicate to the MD2 in a proper way, ERROR 2 is shown in the display of the DST. Trying again by changing the DST position a little bit might often help.
- If the error buffer of MD2 is empty, no errors are displayed by the DST; the display remains blank.

6.3.2 *Clearing the error buffer*

The error buffer can be cleared in 2 ways:
1. In the SAM by selecting the item RESET ERROR BUFFER in the main menu.
2. By the 'DIAGNOSE 99' command of the DST (in all modes except the SAM). Press the DIAGNOSE key on the DST, followed by 9 and 9 and then <OK>.

6.3.3 *Error code table*

See page 8.

Remark: If on the DST the text 'ERROR 2' is displayed, this means that the communication from the TV to the DST has failed.

6.4 Protections

6.4.1 *Protection-structure*

The MD2 'Protection Diagram' shows the structure of the protection system. See protection diagram on page 8.

Two micro-processors
The MD2 chassis has two micro-processors. The micro-processor on the SSP is the so called I/O- or standby-processor and also remains active in standby. The supply of the standby(I/O)-processor comes from the main supply, both in normal operation as in standby. The standby (I/O)-processor controls the standby-LED, controls the STANDBY line for switching on and off the main supply and the SLOW DOWN line for switching off the supply of the line-deflection-circuitry. In the diagnose mode the standby (I/O)-processor feeds through the RC5-communication to the main-processor.

The communication between both processors happens via I^2C. An additional STROBE-line takes care for addressing of the standby(I/O)-processor as the standby(I/O)-processor does not have a defined I^2C address.
Whether the main-processor is OK, is checked by the MAIN-IS-ALIVE-line. This line also gives an indication whether the +5V2 voltage is present. Via this line also transfer of error codes takes place to prevent that a blocked I^2C bus could avoid this transfer.

The communication between the diagnose-information of the Dealer Service Tool (diagnose mode) goes via an IR service LED which is connected to the main-processor. This means that in case of protection the power supply and the main-processor must be switched out their standby mode in order to transfer diagnose-information. After calling the error codes from the error buffer (via the DST), the standby(I/O)-processor shortly starts up the main-supply and the main-processor, after which the main-processor sends the codes to the IR service LED. After the transfer the main-processor and the power supply return to their previous mode (in case of protection the power supply will return to standby mode and the main-processor will be switched off again).

Different protection-levels
Via the Series Switch TS7470 the supply of the line-deflection stage can be switched off and on. Normally (during start-up and switch off) the Series Switch TS7470 is controlled by the SLOW DOWN signal from the standby (I/O)-processor, but in case of an Urgent Alarm the FAST DOWN switches off the line-deflection stage directly. An Urgent Alarm is given to the main-processor via the PROT-line and an inverter. The PROT-line is high in case it is active (low at the input pin 62 of the main-processor).

The protection-system of the chassis has three different levels:

- False Alarm
  During a short time something is wrong, but further action is not required. Examples are: short absence of frame-synchronisation-pulses for example after a program-switch.

- Real Alarm
  In case something is wrong, but immediate action is not required. The processing takes place by the both microprocessors and can take a few seconds.
  The standby(I/O)-processor switches of the line-deflection stage by - via the SLOW DOWN line - opening the Series Switch TS7470. After that via the STANDBY line the supply is switched off.

- Urgent alarm
  A problem is observed upon which immediate switching off of the line-deflection circuitry is required. Via the FAST DOWN line the Series Switch TS7470 is opened. In case the protection-situation remains present after 5 x testing (after 200ms, 400ms, 600ms, 800ms and 1000ms), in that case the main-processor takes over the processing as a 'Real Alarm'; the main-processor places information in the error code buffer and the standby(I/O)-processor switches off the power supply.

An 'Urgent Alarm' can be activated by the East-West protection-circuitry or by an short peak in the beam-current (for example after a picture tube discharge (flash)).

6.4.2 Protection via the DDP (IC7315 on the DDP panel)

The protection output of the DDP is connected to the PROT-line via D6320. Only in case this protection is still active after 5 x testing (every 200ms), the main-processor orders the standby(I/O)-processor to switch off the line-deflection-circuitry (via the SLOW DOWN) and the power supply via the STANDBY command.

Just before switching off, the status register of the DDP is read out and the corresponding error is placed in the error code buffer together with error 48 (Protection). To indicate the protection-situation the stand-by LED starts blinking fast. Via the DST the error buffer can be read.

In case the DDP makes the PROT-line high, the status register of the DDP contains information concerning the reason of the protection. After the main-processor has read the status register via I^2C, the PROT-line will be reset and the status register erased. In case the error repeats, the PROT-line becomes high again and the status register is filled again.

The DDP can detect 3 errors:
- Horizontal Failure: HFB pulses do not have the right shape or are not present (error 69).
- Vertical Failure: VFB pulses do not have the right shape or are not present (error 70).
- EHT overcurrent: Too high beam current (EHT-info) (error 71).

If the DDP does not communicate any more with the main-processor, the main-processor places error 18 in the error buffer.

Remark: During the start up the DDP can not check the HFB and VFB. To check the behaviour of the HFB pulses during the start up anyhow, the circuitry around Opamp IC7360 is present (see start up protections).

6.4.3 Start up protections (Series Switch test)

During start up of the set, the Series Switch TS7470 is tested by Opamp IC7360 on the DDP panel. If the Series Switch TS7470 does not function well, error 47 is generated.

The start up procedure is normally processed as follows:
1. Startup of supply voltages (so also +5V and +8V of the DDP)
   → The PROT line becomes high (active) via opamp IC7360 on the DDP panel (output pin 1 of the Opamp IC7360 becomes high in case no HFB pulses are present; this output is coupled to the PROT-line via diode D6334).
2. Approx 800ms after the supply voltages are present, the DDP starts up (HDRIVE) and tries to start the line-circuitry.
   → The DDP measures the presence of the HFB pulses; these pulses should be absent as the Series Switch is still open.
   → Only in case the HFB remains absent, the PROT-line remains high (active).
3. Only in case the PROT-line is still high approx 200ms after starting up the HDRIVE, the software will close the Series Switch TS7470 (so in a correct situation approx 1000ms after the supply voltages are present the Series Switch is closed)
   → The HFB pulses should be present now (so indeed the Series Switch has closed)
4. Only in case the HFB is present (line is OK and Series Switch is indeed closed), the PROT-line becomes low as both the DDP and Opamp IC7360 are receiving HFB pulses.
5. Everything is OK.

Correct situation

B = 5V/div PROT line at 7L11
A = 10V/div (35Vtt) HFB at test point L4
time base = 0.5S/div

In practice:
- In case the Series Switch is closed continuously (so defective), flyback pulses are already present at point 2. As a result the PROT-line already becomes low at point 2 (already 800ms after the supply voltages are present). The main-processor will order the standby(I/O)-processor to switch the power supply to stand-by and places error 47 in the error buffer.
- In case the HFB pulses remain absent after closing the Series Switch TS7470, the PROT-line remains high (points 3). The line circuitry does apparently not start up (well) or the Series Switch does not close. The standby(I/O)-processor will switch the power supply in stand-by after all. Also in this case error 47 is placed in the buffer.

  Attention: Above mentioned means that error 47 is generated in case the line-deflection circuitry can not be start up well. So in case there are problems in the line deflection part during start up, always error 47 will be in the error buffer. Extra errors in the error buffer like error 48 (protection) and error 69 (horizontal failure) indicate that the defect popped up during normal operation.
  After the next first attempt to start up, this will fail and error 47 is added to the buffer. As a result, an error 47 in the error buffer will mostly not be caused by a defective Series Switch TS7470, but has another cause in the line deflection part.

6.4.4 *East-West protection (EW_PROT)*

The East/West protection switches off the Series Switch TS7470 directly via the FAST DOWN signal and diode D6365 on the DDP panel. Because of the FAST DOWN, the Series Switch TS7470 is switched open, no HFB any more and so via the DDP and IC7360 the PROT-line will also become active and so the main-processor can take over the protection-processing. The East/West protection detects a too high current through the East/West power output stage around TS7480.

Note: **A too high current through the East/West stage can be caused by a defective part in the line-deflection circuitry!!!**

The current through the East/West stage is measured on the LSP via 2 precision resistors (R3483 and R3484). In case an error occurs in the line output stage the voltage across these resistors rises. This voltage is fed to the + input pin 5 of Opamp IC7360 on the DDP panel. The - input is connected to a DC-level of approximately 1V1. In case the voltage on the + input of IC7360 (EW_PROT line) becomes higher than 1V1, the output (pin 7) of IC7360 becomes high. The FAST DOWN also becomes high via D6365 and switches off the supply of the line output stage immediately via the Series Switch.
The FAST DOWN is kept high (via D6362) until the power supply is switched into standby (protection) as follows; as the Series Switch is open, no HFB is present any more and so the PROT becomes high by the DDP (error 47 or 48 and 69); after ≥ 1000ms PROT-line high, the protection procedure is started.

As East/west protection does not have a separate error code. Activation of a protection caused by the EW_PROT line can be measured by pin 7 of IC7360 on the DDP. If this pin becomes around 8V for a few seconds, in that case the protection is caused by an activated EW_PROT line.

The East/West protection becomes active in the following cases:

1. Bad contacts in the horizontal deflection circuit:
   * Horizontal deflection coil
   * Linearity corrector coil L5421
   * S-correction capacitor C2432
2. Bad contacts in the flyback capacitor C2425 or C2428
3. Shorted flyback diode D6421.
4. Shortcircuit in E/W transformer (secondary side of T5424 or T5422 (one of the two transformers is present).
5. Shortcircuit in secondary windings of LOT.
6. Shorted S-correction capacitor C2432.
7. Bad solder contacts in the line output stage.
   In case the East/West protection became active, by then the line transistor 7421 can also be defective.

6.4.5 *Software protection*

The software protection is totally managed by the two micro-processors and consists out of a continuous checking on the presence of the +5V2 and the +8V supply voltage and the continuous checking on the activity on the I²C bus.
This checking is done by testing the communication between the two micro-processors and a number of IC's which are connected to this supply voltage. In case one of these IC's do not respond, the protectionprocessing becomes active and the power supply will be switched to stand-by.

+5V2 protection of the standby(I/O)-processor
Via the MAIN-IS-ALIVE line the standby(I/O)-processor checks the presence of the main-processor every 700ms, and after that also the presence of the +5V2 supply voltage.
In case the communication with the mainprocessor fails 3 times after each other, by then the standby(I/O)-processor switches the power supply to standby(I/O) and will blink the standby-LED slowly (1.25Hz). In this case no error code can be written to the error buffer as this is done by the main-processor which does not respond.

+8V protection via the main-processor
The main-processor controls via a number of IC's the presence of the +8V supply voltage on the SSP. This controls is realised via I²C. The following IC's are used for the check of the +8V supply voltage:

- Videocontroller, TDA4780, (error 16)
- Videoprocessor, synchronisation, TDA9141, (error 15)
- Source select, TEA6415C, (error 81)

In case one of the above mentioned IC's does not respond, the error code of that specific IC is stored in the error buffer together with error 45 (+8V error) and the main-processor gives an order to the standby(I/O)-processor to switch the power supply to stand-by.

I^2C protection (error 51)
The (slow) I^2C bus is controlled at each I^2C-command. To do this at every I^2C command a defined start/stop condition is generated. In case this defined start/stop condition fails for a few times after each other, by then error 51 (I^2C error) is placed in the error buffer and the power supply is switched to stand-by.
In case of I^2C protection, the standby(I/O)-processor still can communicate to the main-processor for diagnose mode (reading error codes in the buffer and displaying via the Service LED) by communication via the STROBE line.
I^2C-protection is generated in case the SDA is shorted to earth, in case the SCL is shorted to earth or in case the SDA and the SCL are shorted.

Remark: The (fast) I^2C bus for teletext and the I^2C bus to the EAROM are not checked for protection matters. By the way, both busses are only present on the TXT+control panel (panel with the main-processor).

Flash protection
A special protection is the EHT-info protection. After a 'flash' in the picture tube (a peak current as a result of an internal discharge) this protection switches off the line output stage by the FAST DOWN signal. On the DDP panel the circuitry around TS7390, 7391 en 7392 detects a fast dip in the EHT-info-line. The voltage at this line becomes negative at the moment of a flash. Via the previous called transistors the FAST DOWN line becomes high and so the supply of the line output stage switches off before an increased current can damage the line-deflection circuitry.
As a 'flash' only has a temporary character, the line output stage will start up immediately again. The error is very short and will be denied by the main-processor (false alarm). Within less than 0,5 a second the line circuitry will start up again.

6.4.6 Rest of the protection diagram

The voltages generated by the LOT
The line output stage generates different secondary voltages:
- +13VLOT to the picture tube panel (pin 8 of the LOT);
- -15VLOT to the DDP and the picture tube panel (pin 9 of the LOT);
- The filament (heating) of the picture tube (pins 11 and 12);
- The +200V for the RGB output stages (pin 7);
- The supply of the DC shift circuitry (pins 4 and 7);
- The EHT is generated by a diode split. The focus and the VG2 voltage are derived from the EHT. The focus and VG2 potentiometers are integrated in the line output transformer (LOT).

The beam current flows from the 141V through R3450 and 3451. In case of an increasing beam current, the voltage at pin 10 of the LOT and so the voltage across C2450 will decrease.

6.5 Faultfinding and repair tips

See faultfinding trees on page 8.

6.5.1 General

1. With most defects the MD2 will give no picture and no sound; the set is in protection (power supply switched to standby, so the entire set is down except the standby(I/O)-processor.
2. **LED indication after start-up procedure is completed (see fault finding tree):**
   - No LED's
     Supply or microprocessor problem.
   - Both LED's continuously
     Control part or standby mode defective.
   - Red LED blinking slow (1.25Hz)
     Protection mode (main proces sor or +5V2).
   - Red LED continuously
     Control part, RC or RC5 defective.
   - Red LED blinking fast (5Hz)
     Protection mode (all other errors).
   - Green LED continuously
     Supply and micro-processors are OK.

   Switch on the set via the mains-switch.
   If the LED's behave properly it is likely that the microprocessor is OK.
   The green LED shows that the power supply has started up. If, after a few seconds, the stand-by LED is blinking an error is detected. Now the supply is switched to stand-by position again. Restart is only possible via the mains-switch or the internal service pins.
3. Audible checks:
   - Do you hear demagnetisation? Yes, mains voltage is present at mains input panel.
   - Do you hear EHT? Yes, supply is OK (DDP and line output stage only works in case VOS (141V) is OK).
   - Power supply is hiccuping? Power supply is shorted. Check the LOT, Series Switch TS7470, line transistor TS7421.
4. Error codes
   In case error 48 is displayed, the protection circuit was active and initiated by the PROT-line. Reading the next error code can give other information about the defect. If, for example, the second error is 69 H-FAIL (detected by the DDP because the HFB pulses do not have a correct shape) we know that the line circuit is not working properly.
   Error 18 indicates that the DDP does not communicate to the main-processor. Most likely the power supply is not working or short circuited.

   Some important error buffer possibilities:

44 47	Line error occurred at/before start up
44 48 69	Line error occurred during normal operation
47 44 48 69	Line error occurred during normal operation and after that a try for start up again was performed.

   Line errors can be:
   - ★ Series switch test (this error can only be generated at start up)
   - ★ East/west protection (EW_PROT)
   - ★ HFB fail

   See paragraph 6.5.3 for a faultfinding method within the line output stage.

44 48 70	Frame error (error can occur at/before start up or in normal operation)
44 48 71	EHT-INFO problem, so eg +200D not present or one of the RGB amplifiers is shorted (error can occur at/before start up or in normal operation)
44 (45) 51 82	I^2C bus shorted, or SCL is shorted or SDA is shorted. In case of such I^2C-problems, the error buffer always shows 44 51 82 after erasing the error buffer and then start up again.
5. Overrule start up protection (error 47) and +8V protection (error 45)
   While the set is in the protection mode (power supply in standby), start the SDM or SAM via the service pins at the component side of the SSP.
6. Microprocessor problems
   In case of microprocessor problems, via the shape of the MAIN_IS_ALIVE it can be determined whether the main-processor, the standby(I/O)-processor or the +5V2 has caused the problem. The MAIN_IS_ALIVE must be measured at pin 36 of the standby(I/O)-processor.

Protections, Faultfinding and Repair tips

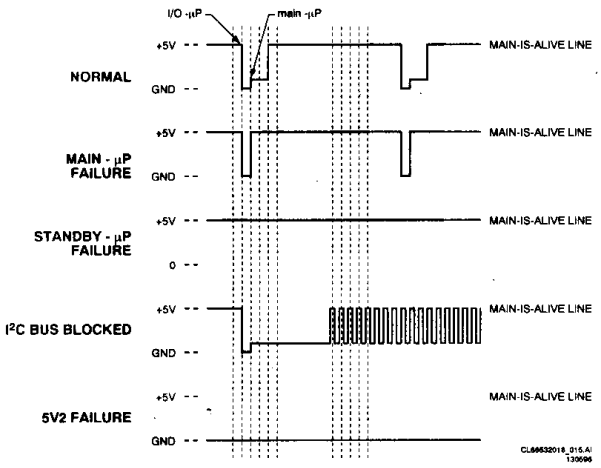


Fig. 6.5

So:

a Pulses without 0V3 steps
→ main-processor failure

b Always 5V2, so no pulses at all
→ standby(I/O)-processor failure

c Always 0V, so no pulses at all
→ +5V2 not present

7. Dolby
In dolby sets, both the clickfit and the surround sound panel can be bypassed (taken out) by connecting the speaker plug in L38 in stead of U36.

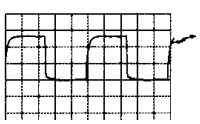
6.5.2 *Fault finding in the power supply*

In case of a power supply problem, the power supply can be simplified to a stand alone power supply at low voltages (low risk) as follows:

Control part of the power supply

1. Disconnect the SSP (as a result the line will not function any more, so will not be a load of the power supply any more) or disconnect the line by jumper 9471 on the LSP.
2. Connect an external DC power supply between supply pin 1 IC7520 (via a diode - eg BYD33D - with cathode to supply pin 1 IC7520) and hot earth (e.g earth of the big smoothing capacitor C2505)
3. Connect a oscilloscope to test point P5 at pin 3 IC7520.
4. Turn up the external DC supply voltage slowly to 17V DC.
Remark: The IC starts at a supply voltage of approx 14V DC, after that the supply voltage can drop to approx 9V DC.
At approx 18V DC, overvoltage protection becomes active, by then the supply voltage should first drop below 7V DC before a new start-up is performed by turning up the supply voltage above 14V DC.
5. In the correct situation the oscillogram should be as displayed below. If not the power supply control part (IC7520 or periphery at pins 9, 10 or 11) is defective.

A = 5V/div
time base = 5µS/div
→ 40kHz pulse

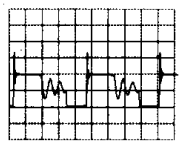


Energy transfer of the power supply (only if control part is OK)

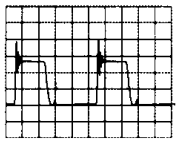
6. Apply action 1, 2 and 4 (if not already done)
7. Connect a lamp of 220V 100W across the VOS output capacitor C2569.
8. Connect a 1k resistor between the +8S (connector 4L10) and the STANDBY line (between R3595 and R3596) to switch the power supply to normal operation.
9. Connect the mains to a VARIAC but leave it at 0
10. Connect a voltmeter across C2569 and a scope between the drain of TS7541 and hot earth.
11. Slowly increase the mains input voltage by the VARIAC (in this way further damage to the power supply can be avoided).
The oscillograms for the following mains voltage are given:

Mains in voltage
10V AC: 20kHz and VOS 7V5
20V AC: 40kHz and VOS 30V
40V AC: 40kHz and VOS 80V
65V AC: 40kHz and VOS 140V
>65V AC: Stable situation, so 40kHz and 140V

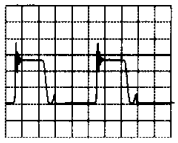
1. Mains in 10V AC
A = 10V/div
time base = 10µS/div
→ 20kHz pulse
→ VOS 7V5



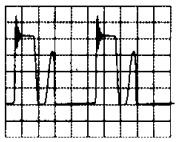
2. Mains in 20V AC
A = 20V/div
time base = 5µS/div
→ 40kHz pulse
→ VOS 30V



3. Mains in 40V AC
A = 50V/div
time base = 5µS/div
→ 40kHz pulse
→ VOS 80V



4. Mains in 65V AC
A = 50V/div
time base = 5µS/div
→ 40kHz pulse
→ VOS 140V



A more detailed fault finding tree for this power supply is given in the MD1 service manual and service informations. Note in this respect that the MD2 power supply is principally the same as the MD1 25-28" power supply (so not the same as the MD1 21" power supply).

6.5.3 *Fault finding in the line circuitry*

The HFB (test point L4 or between C2419 and C2420) together with PROT line (eg at connector 7L11) are very informative test points for possible line circuitry faults.
A good way of working is:

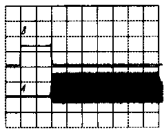
A. Check DDP (HDRIVE);
B. Check the HFB and the PROT lines in a normal set-up (220V mains and HDRIVE via DDP);
C. Second, in case the problem is in the line circuitry itself, the line circuitry can be simplified to a stand alone 'switched mode supply' at low voltages (low risk).

HFB and PROT measurements at start up in a normal set-up (220V mains and HDRIVE via DDP)

1. Connect a oscilloscope to the PROT signal (connector 7L11) and the HFB test point L4 (for a stable oscilloscope pattern, trigger the scope at the rising or falling edge of the PROT signal and apply a delay if needed).
2. In case of line problems normally the set is in protection. All test given below are done during the start-up phase, so the protection behaviour can be observed. After every new test, leave the set a few seconds enabling it to reset the protection.

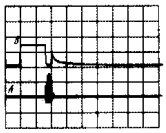
Possibilities:

1. B = 5V/div PROT line at 7L11
   A = 10V/div (35Vtt) HFB at test point L4
   time base = 0.5S/div



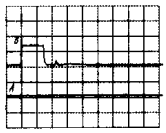
   So 1000ms PROT high (8V), then HFB continuously
   → **Correct situation**
   See paragraph 6.4.3

2. B = 5V/div PROT line at 7L11
   A = 10V/div (35Vtt) HFB at test point L4
   time base = 0.5S/div



   So 800ms PROT high (8V), then 200ms HFB
   → **Series Switch shorted**
   Note: Amplitude OK (35Vtt), so line circuitry is OK. Directly after mains switch on after approx 800ms pulses appear for approx 200ms followed by protection.
   See also paragraph 6.4.3; As the Series Switch is shorted, already after 800ms HFB pulses are present and the DDP will make the PROT line low. Because the PROT line is already low after 800ms, the set will switch into protection mode.

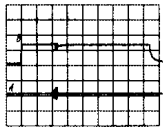
3. B = 5V/div PROT line at 7L11
   A = 10V/div (35Vtt) HFB at test point L4
   time base = 0.5S/div



   So 4 seconds PROT high (8V) and no HFB
   → * **Series Switch open or**
   * **line transistor open or**
   * **no HDRIVE**
   See also paragraph 6.4.3; After 1000ms the processors tries to close the Series Switch, but this is defective (open) and so there will be no HFB pulses measured at the DDP. In that case the software will wait for another 3000ms for HFB pulses. If this pulses will not be there even after this 3000ms, the set will switch into protection.

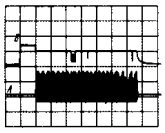
4. HFB and PROT both at zero during start up.
   Power supply is shorted, so power supply hiccup and has no output voltage.
   → **Series switch and VOS (eg line transistor TS7421 or both diodes D6421 and 6422) shorted.**

5. B = 5V/div PROT line at 7L11
   A = 10V/div (35Vtt) HFB at test point L4
   time base = 0.5S/div



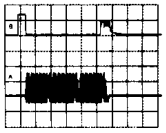
   So 4 seconds PROT high (8V) and shortly a HFB
   → * **Series switch, line transistor and HDRIVE are OK**
   * **No line deflection (eg horizontal deflection coil not connected or open)**
   See also paragraph 6.4.3; After 1000ms the Series Switch is closed, but the HFB is not correct. The small oscillation at 32kHz made 'somewhere in the line' indicates that the Series Switch, the line transistor and the HDRIVE are OK.

6. Two phenomema's:
a No picture, no sound; after approx 5 seconds very shortly a horizontal line and then the set switches into protection
b B = 5V/div PROT line at 7L11
   A = 10V/div (35Vtt) HFB at test point L4
   time base = **1S/div**



   So in case of a horizontal line for a very short moment and in case for 1 second PROT high (8V) and no HFB and then for 7 seconds PROT high (5V) and HFB
   → **No frame deflection (eg frame deflection coil not connected)**
   Start up procedure (1000ms PROT at 8V) is OK. After that the Series Switch is closed. In this case HFB pulses are normal present, but as the VFB pulses are not present (DDP generates error 70 V_FAIL) the PROT line becomes active driven by the DDP (for 7 seconds the PROT will be at 5V driven by the DDP).

7. Two phenomena's:
a Very bright picture with even whiter flyback lines. After approx 10 seconds set switches into protection
b B = 5V/div PROT line at 7L11
   A = 10V/div (35Vtt) HFB at test point L4
   time base = **2S/div**



   So very bright picture with even brighter flyback lines and 1 second PROT high (8V), approx 8 seconds PROT low and HFB pulses and then 1 seconds PROT high (5V) with HFB
   → * **No +200D heater voltage**
   * **RGB amplifiers shorted**
   Start up procedure (1000ms PROT at 8V) is OK. Approx 8 seconds after this start up procedure, the DDP will make the PROT high (5V) because the EHT-INFO is too high (DDP will generate error 71 Overcurrent). After 1 second PROT high the set will go to protection.

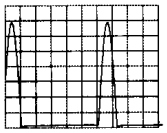
In case the line circuitry itself is defective

In case the line circuitry itself is defective, the line circuitry can be simplified to a stand alone 'switched mode supply' at low voltages (low risk) as follows:

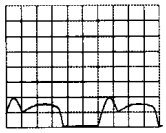
1. Take out the mains connector;
2. Disconnect the SSP;
3. Connect an external 50V DC (or 40V DC) supply with current measurement possibility between the source (output side) of the Series Switch TS7470 and ground;
4. Replace the DDP HDRIVE by an external LF generator (TTL level, so between 0 and 5V and duty cycle 50%) with a 32kHz pulse at cathode of D6409 (near LOT at the side of the PCB);
5. Connect a oscilloscope to test point L1 (collector of line transistor TS7421).

Possibilities:

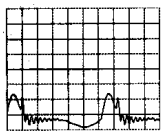
1. A = 50V/div test point L1 at collector line transistor
time base = 5µS/div
Current from external DC supply approx 100mA
So normal 32kHz pulses and 100mA supply current
→ Correct line circuitry
Amplitude of the signal is strongly depending on the frequency of the generator



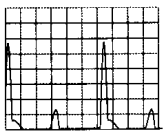
2. A = 50V/div test point L1 at collector line transistor
time base = 5µS/div
Current from external DC supply approx 100mA
So lower pulses followed by long pulses and 100mA supply current
→ Line deflection open, so eg:
   * **line deflection coil open**
   * **linearity coil L5421 open**
   * **S-correction C2432 open**



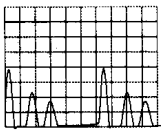
3. A = 50V/div test point L1 at collector line transistor
time base = 5µS/div
Current from external DC supply approx 500mA !!
So fast oscillations and 500mA supply current
→ Line deflection shorted
(eg line deflection coil shorted)
In case the line deflection is not completely shorted, but only a number of windings are shorted, the oscillogram is there without the oscillation and a current of the external DC supply of approx 200mA.



4. A = 100V/div test point L1 at collector line transistor
time base = 5µS/div
Current from external DC supply approx 150mA
So flyback time is shorter, one extra pulses in between, 150mA supply current
→ Flyback C2425 open



5. A = 100V/div test point L1 at collector line transistor
time base = 5µS/div
Current from external DC supply > 1A
So 2 pulses per cycle extra and supply current from more than 1A
→ Short in picture tube
(eg EHT to aquadag)



6.5.4 Fault finding in the sync part (see also fault finding tree)

1. Antenna out and TXT/OSD-menu is stable (OK)
   * DDP and line seems to be OK
   * Probably synchronisation problem in the video processor (HA, VA) or Feature Box (HD, VD)
2. Antenna out and TXT/OSD-menu is not stable (scrolls)
   * No synchronisation at all, so DDP or line problem

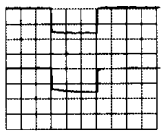
6.5.5 Fault finding no picture and no protection LED → problem in the video controller (TDA4780) part

In case there is no picture and no protection, most likely there is a problem with the BC_INFO (TDA4780 or RGB amplifiers or picture tube).

Normal start up procedure:
Connect a video generator (eg PM5518) with a white pattern to the tuner and trigger the oscilloscope field frequent (a more stable picture is obtained if triggered at VD of the Feature Box; pin 6 S48).

1. First phase of start up; 4 white measuring lines (lines 15, 16, 17, 18) and the main picture is muted (these oscillograms are best visible if the picture tube is cold);

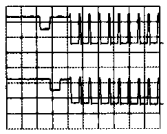
Red and green (or blue) gun
100V/div DC
50µs/div
4 measuring lines white



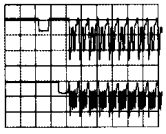
Total beam current is measured and feedback to pin 19 TDA4780.
The TDA4780 checks whether the voltage at pin 19 TDA4780 (IC7500) is ≥ 4V5 (during these lines)
Yes → go to phase 2
No → remain in phase 1

2. Second phase of start up; each beam separately is measured and the main picture is still muted. Line 15 is Red, line 16 is Green and line 17 is Blue. By now BC_INFO is measured:
   * Differences are compensated
   * If differences are minimal then go to phase 3

Red (line 15) and green (line 16) gun
50V/div AC
50µs/div



Red (line 15) and blue (line 17) gun
50V/div AC
50µs/div



Faultfinding and Repair tips

3. After start up the picture is present and differences in cut-off points of the R, the G and the B gun are compensated continuously

Repair procedure

In case of no picture and no error codes
- Switch on the set
- In a 4x3 set, press compress (16:9)
- In a 16x9 set, shift down the picture

Now you can see in which start up phase the set is:

1. **A bright white line** (first phase of start up procedure)
   → there is a monitor pulse, so the TDA4780 + picture tube + RGB amplifiers are OK
   → there must be 4V5 feedback at pin 19 TDA4780
   → If no 4V5 fault in feedback loop

2. **Small R and G and B lines**
   (second phase of start up procedure)

   TDA4780 is OK

   Probably one gun of the picture tube is bad
   → Measure at pin 19 TDA4780 which feedback line (the R or G or B line) is less; the corresponding gun is wrong (amplifier or gun)

3. **No lines visible**
   Measure pin 19 TDA4780
   - 0V — Check TDA4780 (sandcastle and the supply voltage)
   - 5V — Check RGB amplifiers
     Short pin 19 TDA4780, now there will be measuring lines
     (at continious 5V phase 1 and 2 are bypassed)
   - Pulses — there is a measure line, so the TDA4780 is OK
     Measure on cathode on the CRT panel if the measure lines are present:
     Yes → BC_INFO circuit is open or no HEATER voltage
     No → RGB amplifier problem

8. Electrical adjustments

General alignment conditions

All electrical adjustments/alignments should be made under the following conditions:

* Power supply voltage: 220-240V ± 10%; 50-60 Hz ± 5%.
* Warm-up time ≈ 10 minutes.
* Voltages and oscillograms are measured in relation to tuner earth (with exception to the voltages on the primary side of the power supply). **Never** use the cooling fins/plates as earth.
* Test probe: Ri > 10 MΩ; Ci ≤ 20 pF.

8.1 Large signal panel adjustments [A]

8.1.1 +141V power supply voltage

- Connect a voltmeter to the positive side of C2569.
- Using **R3559** adjust the power supply voltage to +141V ± 0V5.

8.1.2 Focusing

This is adjusted using the focus potentiometer (uppermost on the line transformer).

8.1.3 Vg2 adjustment

- Use the Service Alignment Menu to switch on the Vg2 test pattern (see paragraph 8.4).
- With the aid of a DC voltmeter (Ri > 1MΩ) measure the DC voltages on pins 8 of the RGB output amplifiers IC7330, IC7340 and IC7350 on the picture tube panel.
- Determine the highest of the three voltages using the Vg2 (SCREEN) potentiometer on the line output transformer and adjust it to 155V ± 2V.

8.1.4 Horizontal centring (DC offset)

- Use the Service Alignment Menu (see paragraph 8.94) to switch on the geometry test pattern and then select in sequence: Alignments, Geometry, Test pattern on, H-Shift.
- Use H-Shift to adjust the picture in such a manner that the test pattern appears in the middle of the picture tube (video centrallin in the deflection window).
- If the adjustment range of the H-Shift is insufficient, the deflection window can be moved using the jumpers on the DC-shift panel.
- If the DC-shift panel is used the video must then be placed in the middle of the deflection window again via H-Shift.

Remarks:
The 'Horizontal Shift' adjustment in the Service Alignment Menu **cannot** be adjusted using the internal test pattern. An external test pattern from a generator or an aerial is required for this purpose.

8.2 Small signal panel adjustments [K]

8.2.1 Y/CVBS level

- Feed in a CVBS grey scale signal with a nominal amplitude (between black and white) to pin 20 of EXT1 and select the picture on EXT1.
- Use **R3503** on the SSP to adjust the amplitude of the signal to 345mV$_{pp}$ (between black and white) on pin 8 of IC7500 (TDA4780) on the SSP (K).

8.3 TXT + control module [J3] adjustments

8.3.1 24 MHZ crystal for Text DualScreen

- Select a programme using teletext.
- Activate the Text DualScreen mode.
- Adjust **L5465** so that the teletext half is stable on the screen and when turning to both the left and right some margin remains.

8.4 IF module adjustments [L]

8.4.1 AGC (Automatic Gain Control) take-over point adjustment

Rough adjustment:
- In case the picture from a local transmitter is distorted, adjust the AGC using **R3140** until the picture is no longer distorted.

Fine adjustment:
- Connect a video generator (e.g. PM5518) to the aerial input.
- Select a 475.25 MHz colour bar without sound.
- Set the video generator to its highest level.
- Select the Service Default Mode by means of the <DEFAULT> key on the DST or by briefly shorting the SERVICE DEFAULT MODE pins.
- Connect an oscilloscope to the output of the tuner (pin 17).
- Adjust the AGC take over point using **R3140** so that the oscilloscope indicates 0.5V$_{pp}$.

8.4.2 AFC (Automatic Frequency Control) adjustment

- Select 'MANUAL' adjustment in the installation menu.
- Select a transmitter frequency of 175.25 MHz (upper left on the screen) by means of the digit keys and the PROGRAM +/- keys. Once the frequency has been accurately adjusted using PROGRAM +/-, the set is forced to that frequency and the AFC adjustment is switched off.
- Connect a video generator with a colour bar and a frequency of 175.25 MHz to the aerial input.
- In a 'Multi West Europe' set (-/12) select system BG on the video generator and system 'WEST-EUROPE' in the installation menu.
- In a 'Multi French' set (-/05/19) select system L on the video generator and system 'FRANCE' in the installation menu.
- In a 'Multi East Europe' set (-/58) select system DK on the video generator and system 'EAST-EUROPE' in the installation menu.
- Connect a multimeter to the AFC output on pin 12S59.
- Use **L5165** to adjust the AFC to 2V6.

8.4.3 34.4 MHz adjustment for 'Multi West Europe' (BGLM -/12) and 'Multi East Europe' (BGLMDK -/58) sets

- Select a program with system 'AMERICA' or go to the installation menu and make a program with system 'AMERICA'.
- Connect a video generator to the aerial input.
- Select system NTSC M with 1kHz sound and a fully black picture.
- Connect an oscilloscope to connector 10S59 (CVBS_TERR) and trigger line-frequent.
- Adjust the 34.4 MHz filter using **L5101** so that the sound carrier wave at 34.4 receives maximum suppression (minimum amplitude of the oscillation).

8.4.4 40.4 MHz adjustment for Multi France sets (BGLL'I -/05/19)

- Select a program with system 'FRANCE', but not a program in the VHF1 band (so select a SECAM L transmitter).
- Connect a video generator to the aerial input.
- Select system SECAM L with 1kHz sound and a completely black picture.
- Connect an oscilloscope to connector 10S59 (CVBS_TERR) and trigger line-frequent.
- Turn the 40.4 MHz TOKO **L5102** fully to the right.
- Now turn the TOKO slowly to the left until:
  - ★ the amplitude of the subcarrier begins to increase, or
  - ★ peaks appear in top of the signal.

8.5 Audio Power Supply Module adjustments [AB]

8.5.1 +16V supply voltage

- Connect a voltmeter to the positive side of C2307.
- Switch off the load (mute the sound).
- Using **R3311** adjust the supply voltage to +16V5.

8.6 VDS adjustment (Video DualScreen) module [AC]

8.6.1 AGC (Automatic Gain Control) transfer point adjustment

Coarse adjustment:

- If the picture of a local transmitter is distorted, adjust the AGC using **R9H5** until the picture has no distortion.

Fine adjustment:

- Connect a video generator (e.g. PM5518) to the aerial input.
- Select a colour bar at 475.25 MHz without sound.
- Drive the video generator to full power.
- Select the Service Default Mode using the <DEFAULT> key on the DST or by briefly short-circuiting the SERVICE DEFAULT MODE pins.
- Select VDS mode and select on the right-hand screen the same programme as on the left-hand screen.
- Connect an oscilloscope to the tuner output (pin 17).
- Using **R9H5** adjust the AGC transfer point so that the oscilloscope reads $0.5V_{pp}$.

8.6.2 AFC (Automatic Frequency Control) adjustment

- Switch off the VDS mode and select 'MANUAL' tuning in the installation menu of the main screen.
- Select a transmitter frequency of 175.25 MHz (top left in the screen) using the digit keys and the PROGRAM +/- keys. As soon as the frequency is set accurately using the PROGRAM +/- the main and, as a result of this, the VDS tuner, are forced to that frequency and the AFC control is switched off.
- Save these settings and exit the installation menu.
- Connect a video generator with a colour bar and a frequency of 175.25 MHz to the aerial input.
- Select system BG on the video generator and system 'WESTERN EUROPE' in the installation menu.
- Select VDS mode and on the right-hand screen select the same programme as on the left-hand screen.
- Connect a multimeter to the AFC output on pin 23 of IC9R (IF modulator of the VDS modules).
- Using **L9F7** adjust the AFC to 2V6.

8.6.3 40.4 MHz adjustment for (BGLL'I)

- Select a programme with system 'FRANCE', however, not a programme in the VHF1 band (therefore select a SECAM L transmitter), for example 475.25 MHz.
- Connect a video generator to the aerial input and select system SECAM L with 1 kHz sound and a full black picture.
- Select VDS mode and on the right-hand screen select the same programme as on the left-hand screen.
- Connect an oscillioscope to connector pin 10 of IC9R (TUN_CVBS) and trigger line frequency.
- Turn the 40.4 MHz TOKO **L9F2** fully clockwise.
- Now turn the TOKO slowly anticlockwise until:
  - ★ the amplitude of the subcarrier starts to increase or
  - ★ peaks are created on the top of the signal.

8.7 Wireless Dolby transmitter and receiver adjustment [AE]

8.7.1 Maximum FM frequency sweep adjustment of the transmitter [AE1]

Fine adjustment with an FM frequency sweep meter:

- Connect a signal generator to the input of the transmitter (pin 1 or 3 of plug 1409).
- Select 1 kHz 600 mV top-top signal.
- Using an FM frequency sweep meter measure the aerial output of the transmitter.
- Using **R3442** adjust so that the FM frequency sweep is 75 kHz.

Coarse adjustment without FM frequency sweep meter:

- Use the wireless Dolby transmitter and receiver.
- Select the same channel for both.
- Connect a signal generator to the input of the transmitter (pin 1 or 3 of plug 1409).
- Select a 1 kHz 600 mV top-top signal.
- Connect a multimeter to pin 2 of plug 1792 on the receiver module.
- Adjust **R3442** on the transmitter to 280 mV top-top on the receiver.

8.7.2 FM detector adjustment of the receiver [AE3]

Fine adjustment with a signal generator with FM frequency sweep control:
- Connect a signal generator to the input of the receiver 1710
- Select a 433.750 MHz signal with 1 mV top-top and a FM frequency sweep of 75 kHz
- Connect an oscilloscope to the anode of C2772 (T716)
- Adjust **L5710** to minimal distortion

Coarse adjustment with a pattern generator:
- Use the wireless Dolby transmitter and receiver
- Select the same channel for both.
- Connect a signal generator to the input of the transmitter (pin 1 or 3 of plug 1409).
- Select 1 kHz signal.
- Adjust **L5710** to minimal distortion.

8.7.3 Pilot tone adjustment of the receiver [AE3]

Fine adjustment with a signal generator:
- Connect a signal generator to the input of the receiver 1710.
- Select a 433.750 MHz signal with 1 mV top-top without FM frequency sweep.
- Connect an oscilloscope or a frequency counter to the test point T731 close to pin 13 of IC7710.
- Adjust **R3721** to 76 kHz.

Coarse adjustment with pattern generator:
- Use the wireless Dolby transmitter and receiver.
- Select the same channel for both.
- Connect a signal generator to the input of the transmitter (pin 1 or 3 of plug 1409).
- Select a 1 kHz signal.
- Adjust **R3721** to the centre of the range in which the receiver clicks on (stereo indication on pin 7 of IC7710 becomes active (low)).

8.8 VGA module adjustment [AF]

8.8.1 Two methods:

- With a video card for which the horizontal frequency is adjustable. Adjust **R3162** such that when the horizontal frequency is above 33.1 kHz, the SVGA detection on the OSD becomes active (32KHZ_DETECT then also becomes 'high').
- Using a signal generator (e.g. PM5326) apply a pulse with a low duty-cycle to the H(PLL) input pin 4 of IC7160 and adjust the frequency to 33.1 kHz. Adjust **R3162** such that at a horizontal frequency above 33.1 kHz, the SVGA detection on the OSD becomes active (32KHZ_DETECT then becomes 'high').

8.9 Adjustments in the Service Alignment Menu; General

Switch on by:
- briefly shorting the service pins 'SERVICE ALIGNMENT MODE' on the SSP;

or:
- pressing the <ALIGN> key on the Dealer Service Tool (DST) (RC7150), followed by keying in the password 3140 and then pressing the <OK> key.

The Service Menu will now appear on the screen.
The following information is now displayed:
1. The software date ('Date') and version ('ID.') of the ROM.
2. The accumulated total of operation hours ('Operation Hours').
3. The contents of the error buffer ('Errors') (the most recent error displayed at the upper left, immediately following 'ERRORS'; see chapter 6.3).
4. The module generating the error ('Defect. Module') (if there are multiple errors in the buffer that have not all been generated by a single module, there is probably another defect. The message 'INDETERMINATE' will then be displayed here).
5. Menu item 'Reset Error Buffer'. The error buffer can be reset by pressing the <OK> key.
   Menu item 'Functional Test'. All devices are tested via the <OK> key. Eventual errors are displayed in the error buffer (the error buffer is not erased; the contents return when the Functional Test is terminated).
7. Menu item 'Alignments'. This enables the Alignments sub-menu to be called up.
   The following alignments can be selected:

   'General':
   Adjustment of 'White Drive', 'Cut-off', 'Vg2 test Pattern', 'Peak White Limiter','PIP brightness'.

   'Normal Geometry':
   General geometry adjustments.

   'Super wide geometry':
   Geometry adjustments for the 'Panorama' position in 16:9 sets.

   'Options':
   Setting the initialisation codes in the set via text.

   'Option number':
   All options together, expressed in two long numbers. The original factory setting for these numbers can be found on the picture tube sticker on the inside of the set.

   'Store':
   Store all adjustments.

The adjustments
General:
* Once all alignments/adjustments have been completed the item 'STORE' must be selected to record all the values in permanent memory.
* When the option codes have been changed and stored the set has to be switched on and off using the mains switch to activate the new settings (when switching on and off via stand-by, the option code settings are NOT read by the microprocessor).
* If an empty EAROM (permanent memory) is detected, all settings are set to pre-programmed standard values.
* A built-in test pattern can be called up in various sub-menus. The test pattern generator can be switched on using the item 'TESTPATTERN ON/OFF'. The test pattern only appears AFTER the specific alignment/adjustment has been selected.
  The test patterns are generated by the teletext module.

Electrical adjustments

8.10 Picture tube adjustments in the Service Alignment Menu

8.10.1 'White Drive'

- For the first adjustment turn off DNR and 'Contrast Plus'.
- Use the internal test pattern (a white picture). Adjust the white level for the three settings 'WARM', 'NORMAL' and 'COOL'.
- Start in the 'NORMAL' position and take the standard values for green, red and blue as a starting point (value 50) and then adjust red and blue.

The following default values are maintained for the 'white drive' settings:

	Cool	Normal	Warm
R	41	42	45
G	37	36	35
B	30	25	19

8.10.2 'Cut-off'

- Before adjusting turn off DNR and 'Contrast Plus', set brightness to step 37 (Brightness: ▬▬▬▬▬▮▮▮▮▮▮) and the contrast setting to maximum.
- Use the internal test pattern (a black picture).

The following default values are maintained for the 'cut-off' settings:

	Cool	Normal	Warm
R	25	30	40
G	24	28	34
B	31	25	20

If the adjustment is (much) too low the set may start flashing.

8.10.3 'Peak White Limiter'

For all of the above mentioned picture tubes a default value of 28 can be maintained for the 'Peak White Limiter'.

8.11 Small signal adjustments in the Service Alignment Menu

PIP brightness
Adjust 'PIP brightness' in such a manner that the brightness of the PIP picture is the same as the brightness of the main picture.

8.12 Geometry adjustments 'Normal Geometry' in the Service Alignment Menu

8.12.1 Vertical amplitude and centring

Select 'Test Pattern on'.
a. Adjust the vertical amplitude using 'V amplitude' so that the test pattern is fully visible.
b. Adjust the vertical centring using 'V shift' so that the test pattern is located vertically in the middle.

Repeat the adjustment of 'V amplitude'.

8.12.2 Vertical linearity

Select 'Test pattern on'.
Adjust the vertical linearity using 'V linearity' so that the top and bottom of the picture has equal amplitude.

8.12.3 Vertical S correction

Select 'Test pattern on'.
Adjust the vertical S correction using 'V S-correction' so that the vertical amplitude at the top of the picture is equal to the amplitude in the middle of the picture.

8.12.4 Horizontal centring and amplitude

Select 'Test pattern on'.
a. Using 'H amplitude' adjust the horizontal amplitude so that the entire test pattern is visible.
b. Feed in an external test signal.
Use 'H shift' to adjust the picture horizontally in the middle.

Repeat the 'H amplitude' adjustment if necessary.

8.12.5 East/west adjustment

Select 'Test pattern on'.
a. Use 'East/West parabola' to adjust the vertical lines until straight.
b. Use 'East/West corner' to adjust the vertical lines in the corners until straight.
c. Use 'East/West Trapezium' to adjust the picture until rectangular.
d. If necessary select 'East/West Top compensation' and adjust as required.

Repeat steps 8.12.5a to 8.12.5c if necessary.

8.13 Geometry adjustments 'Super wide geometry' in the Service Alignment Menu

Only applicable to 16:9 sets

8.13.1 Vertical amplitude and centring

Select 'Test Pattern on'.
a. Adjust the vertical amplitude using 'V amplitude' so that the entire test pattern is visible.
b. Adjust the vertical centring using 'V shift' so that the test pattern is positioned vertically in the middle.

Repeat the adjustment of 'V amplitude'.

8.13.2 Horizontal amplitude

Select 'Test pattern on'.
Use 'H amplitude' to adjust the horizontal amplitude so that the entire test pattern is visible.

8.13.3 Vertical S correction

Select 'Test pattern on'.
Adjust the S correction using 'V S-correction' so that the vertical amplitude at the top of the picture is equal to the amplitude in the middle of the picture.

8.13.4 East/west parabola

Select 'Test pattern on'.
Use 'East/West parabola' to adjust the vertical lines until they are straight.

8.13.5 Horizontal centring and amplitude

Feed in an external test signal.
Use 'H shift' to adjust the picture horizontally in the middle.

8.14 Luminance delay

A new adjustment has been introduced with the introduction of the TDA9143 (and TDA9144 in GFL). In the 'GENERAL' menu of the 'ALIGNMENTS' menu the item 'Luminance delays' has been added. These 'Luminance delays' adjustment can only be selected if the set is fitted with a TDA9143 (or TDA9144 in GFL).
If 'Luminance delays' is selected, the following sub-menu appears:

- Luminance Delay Pal
- Luminance Delay Secam
- Luminance Delay Bypass

With the 'Luminance delay' adjustments the luminance information is placed on the chrominance information (brightness is pushed onto the colour).

- The Pal adjustment is only active with Pal signals and must therefore also be adjusted with the Pal signals.
- The SECAM adjustment is only active with SECAM signals and must therefore also be adjusted with the SECAM signals.
- The BYPASS adjustment is only active with NTSC signals, whereby the COMB filter is switched on, and with Palplus signals. Therefore, this adjustment can also only be performed for these signals (if the adjustment for Palplus signals is correct, then this also is automatically good for NTSC signals with COMB filter and vice versa).

As with all other adjustments, here the modified adjustment is only stored after the 'STORE' command.

8.15 Adjustment on the PIP panel in the Service Alignment Menu

PIP AGC adjustment
The AGC adjustment prevents overdriving of the PIP-tuner if the aerial signal is too strong. Overdriving is visible as a loss of colour and synchronisation in the PIP picture. Amplification has to be adjusted to minimum level, but the PIP-picture should be as free of noise as possible.
At maximum amplification **R3912** is turned fully left, at minimum amplification **R3912** is turned fully right.

Adjustment:

- Apply a (strong) aerial signal of 4mV (72dBmV).
- Turn R3912 fully to the right (minimum amplification). Turn R3912 slowly to the left until the noise in the PIP-picture no longer decreases.
- If an aerial signal is not available, compromise by adjusting R3912 to 30% of its total travel (100% is maximum amplification, fully left).

8.16 Option menu

Introduction
The microprocessor communicates with a large number of IC's in the set. To ensure good communication and make digital diagnosis possible, the microprocessor has to know which IC's have to be addressed. The presence of specific IC's or functions is made known by means of the option codes. Only correct option code settings will ensure a correctly functioning set and signalling of the correct error message in case of a defect.
The options have been divided into different groups. These groups contain the various options for which multiple choices are usually possible.

Just as in the beginning of GFL all options which are contained in the set can be manipulated in the MD2.2 Service Alignment Mode using both the option numbers and the OPTION menu.

- All hardware related options are incorporated under the heading 'Options' of the 'Alignments' sub-menu of the 'Service Alignment Mode'.
- All software related options are incorporated under the heading 'Dealer Options' of the 'Service Alignment Mode", but can also be reached directly via the 'DEALER' knob of the DST.

Electrical adjustments

8.16.1 Options in the Service Alignment Mode

Menu name	Subjects	Options	Physically in the set
TV Systems	IF Type	Multi West Europe Multi France Multi East Europe Multi Global BG-only	BGLM set; IF module with L5101 (without junper 4111) (diagram L) BGLL'I set; IF module with L5102 (diagram L) BGLMDK set; IF module with L5101 and jumper 4111 (diagram L) This IF-module is not planned only BG set; IF module without TS7120, 7121, 7123 and 7122 (diagram L)
Stereo Decoder	NICAM	Yes No	Audio IC7353 on Audio Module is MSP3410 (diagram O / P / P2) Audio IC7353 on Audio Module is MSP3400 (diagram O / P / P2)
PIP	PIP Available	Yes No	PIP module present (diagram S) PIP module not present (diagram S)
	PIP Tuner	Yes No	Second tuner PIP U1775 on PIP panel present (diagram S) Second tuner PIP U1775 on PIP panel not present (diagram S)
Teletext	TXT	not available 128 KB 512 KB 1 Mb	no teletext IC7490 is a 128kB (100 pages) teletext memory (code '256' in DRAM typenumber) IC7490 is a 512kB (400 pages) teletext memory (code '400' in DRAM typenumber) IC7490 is a 1MB (800 pages) teletext memory (2 code '400' DRAM's needed which is not possible in MD2.2)
	Level 2.5	Yes No	Level 2.5 TXT (only software related; in MD2.2 always level 2.5 software) Level 1.5 TXT
Communication	Easylink	Yes No	Project 50 (easylink) set No project 50 (easylink) set
Picture tube	CRT Type	4:3 16:9	4:3 picture tube 16:9 picture tube
	Picture Rotation	Yes No	Frame rotation circuitry present (IC7050 diagram G) Frame rotation circuitry not present (IC7050 diagram G)
Video Repro 1	Frame	50/60 Hz 100/120Hz Digital Scan Natural Motion	No Feature Box present Eco Feature Box present (diagram M1) Feature Box 3 present (digital scan) (diagram M1) Feature Box 4 present (digital scan and natural motion with MELZONIC IC7447) (diagram M2)
	Dynamic Contrast	Yes No	SMARTIC IC7008 on the AI module present (diagram N) SMARTIC IC7008 on the AI module not present (diagram N)
	Digital Panorama	Yes No	PANIC IC7010 on the AI module present (diagram N) PANIC IC7010 on the AI module not present (diagram N)
	Auto Format FBX (AARA)	Yes No	Only in 16:9 sets with PANIC IC7010 and SMARTIC IC7008 present on the AI module (diagram N) All other configurations
	Auto DNR	Yes No	LIMERIC IC7006 on the AI module present (diagram N) LIMERIC IC7006 on the AI module not present (diagram N)
	PALplus	Yes No	PALplus panel is present (diagram N2) PALplus panel is not present (diagram N2)
Video Repro 2	Combfilter	Yes No	Comb filter present (diagram Q) Comb filter not present (diagram Q)
	Lum. Trans. Improv.	Yes No	IC7508 TDA9177 present (diagram K) IC7508 TDA9177 not present (diagram K)
	Macrovision Prot.	Yes No	IC7352 is TDA9143 / TDA9144 (diagram K) IC7352 is TDA9141 (diagram K)
	Wide Screen Sign.	Yes No	Wide screen signalling bits for automatic 16/9 selection is enabled (only software) Wide screen signalling bits for automatic 16/9 selection is disabled (only software)
	TXT/EPG DualScreen	Yes No	IC7461, IC7462 and IC7463 present on the TXT+control module (diagram J) IC7461, IC7462 and IC7463 not present on the TXT+control module (diagram J)

9. Ciruit description

Power supply

9.1 Audio power supply

9.1.1 Introduction

In a Dolby set with a sound power of 4 x 15W the power supply of the large signal can deliver insufficient power. Therefore a separate power supply is selected for the sound (+16V and -16V). The so-called 'Audio power supply' is a derived version of the SOPS (Self Oscillating Power Supply) from the FL1-PTV an can supply up to 100W at maximum power.
This SOPS is a mains isolated power supply and the feedback takes place by means of an opto-coupler. Part of the +16V is branched off via potentiometer R3311.
This voltage drives the pulse width controller, which switches on TS7305 and the diode of the opto-coupler earlier or later. This photodiode drives the phototransistor of the opto-coupler in turn, as a result of which switching transistor TS7302 is switched off earlier or later via TS7310 and TS7311.
Since this power supply is a SOPS, it has no fixed operating frequency. The nominal operating frequency is 60 Hz.
The maximum frequency (at Uin = 264V AC and min. load) is 75 kHz. The minimum frequency (at Uin = 198V AC and max. load) is 45 kHz.
The stabilization is achieved by controlling the pulse width.
In standby the power supply is adjusted back to 0V. The power supply is resistant to short-circuit and contains an over-voltage protection.

- *Switching transistor conducts, energy in the transformer*
  When the switching transistor conducts energy is stored in the transformer. The moment that the switching transistor stops conducting is determined by the pulse width controller which monitors the +16V output voltage and the +300V input voltage.
- *Switching transistor reverses, energy from the transformer to the load*
  As soon as the switching transformer reverses, the energy which is in the transformer is transferred to the load. As soon as all of the energy which was in the transformer has been siphoned to the load, the switching transistor starts to conduct again automatically via decay (see self-oscillation).

9.1.2 Pulses on transformer T5305 in normal operation (Fig. 9.1)

As long as the switching transistor is closed, energy is stored in the primary winding 5-1 and supplied to the measuring coupling 8-7:

* As a result of the switching of switching transistor TS7302, pulses with a peak of 900V are induced on pin 5 of the primary winding. This winding is used to store energy in the transformer.
* The positive voltage on pin 8 (+12V) is used as the measuring coupling voltage. This voltage is used to make switching transistor TS7302 conduct extra fast (due to the direction of D6307, winding 8-7 is the only winding which carries current so long as energy is stored in the transformer).

At the moment that switching transistor TS7302 is opened, the energy which is in the transformer is syphoned to the load:

- On the primary side:
  * The winding 9-7 is in phase with the feeding primary winding 5-1. The positive pulse on pin 8 acts as a type of protection which ensures that the switching transistor is unable to conduct as long as there is a high) positive voltage present on pin 5.
- On the secondary side:
  * The positive pulses on pin 22 are rectified and smoothed in order to create the +16V supply voltage.
  * The negative pulses on pin 12 are rectified and smoothed in order to create the -16V supply voltage.
  * The positive pulses on pin 20 are rectified and smoothed in order to create the power supply for the opto-coupler.
  * The negative pulses on pin 14 are used to charge C2312 negatively. This negative voltage on C2312 is used to drive the pulse width controller.

9.1.3 Starting up the power supply during the first 50Hz cycle (Fig. 9.2)

When the first positive half power supply pulse (50 Hz) 'arrives' then via the starting circuit (R3301, R3302, R3306 and L5302) a positive voltage arrives on the base of switching transistor TS7302. As a result of this TS7302 starts to conduct and causes a linear increasing current through primary winding 5-1 of the transformer. This causes the voltage on pin 5 of the transformer to drop and the voltage over the primary winding 5-1 to increase.
Because the voltage over winding 5-1 increases, the voltage over the measuring coupling winding 8-7 also increases causing the voltage on pin 8 to also increase (pin 7 is kept at a constant -5V; see -5V generation). As a result of this an additional starting current is fed back, from pin 8 via C2304 and R3329, with the starting current through R3301 (avalanche effect). This additional starting current runs via 2 routes:

- For rapid changes - in other words during start up - C2304 forms a short-circuit. Therefore the current path C2304, R3329 provides a *short, strong* additional current pulse.
- At the same time a linear increasing positive feedback current flows through D6307 as a consequence of L5303. As a result of this, switching transistor TS7302 conducts more and the voltage on pin 5 drops even faster until the switching transistor is saturated. This current path therefore *maintains* the additional current pulse up to the first self-oscillation (see the description for self-oscillation).

In the event of any breakdown of TS7302 between C and B, the base voltage is limited to 1V8 by means of D6324, D6325 and D6336. As a result of this the transistors on the primary side of the control loop (TS7304, TS7310, TS7311 and TS7315) are protected.

Menu name	Subjects	Options	Physically in the set
Personal	Blue Mute	Yes No	Blue mute active in case of no picture detected Noise in case of no picture detected
	Favourite Programmes	Yes No	Favourite program selection enabled Favourite program selection disabled
	Virgin Mode	Yes No	TV starts up once with language selection menu after mains switch on for the first time (virgin mode) TV does not start up once with language selection menu after mains switch on for the first time (virgin mode)
	Standby Toggle	Yes No	Standby toggle activated; by the standby knob the TV is switched to standby and back to normal operation again Standby toggle de-activated
	Auto Store Mode	none PDC-VPS TXT page PDC-VPS-TXT	Autostore mode disabled (not in installation menu) Autostore mode via ATS (PDC/VPS) enabled Autostore mode via ACI enabled Autostore mode via ACI or ATS enabled
	Multipip	Yes No	Multi-PIP enabled Multi-PIP disabled
	Demo Mode Enable	Yes No	Demo mode enable Demo mode disable
	Auto Format Enable	Yes No	Automatic Aspect Ratio detection (black bar detection) software is enabled Automatic Aspect Ratio detection (black bar detection) software is disabled
	Auto Sharpness Enable	Yes No	Automatic sharpness software is enabled (motion compensation depending on noise level) Automatic sharpness software is disabled
	Auto Motion Enable	Yes No	Auto motion software is enabled (smart keys coupled to nexTView) Auto motion software is disabled
	Auto Smart Control	Yes No	Auto smart control software is enabled Auto smart control software is disabled
	Menu animations	Yes No	Animations at start of menu is enabled Animations at start of menu is disabled
Teletext	Cont. Subtitles	Yes No	Continious subtitles enabled Continious subtitles disabled
	TXT Preference	top flof	Preference to top teletext Preference to flof teletext
	Infoline	Yes No	PDC infoline enabled PDC infoline disabled
	East/West Txt	East West	TXT characters for non -/58 set TXT characters for -/58 set

- If an option selection in the Dealer Mode is not displayed, then that is the result of an option selection in the Service Alignment Mode.
- After the option(s) have been changed, they must be stored via the STORE command.
- The new option is only active after the TV is switched off and then back on again using the mains switch (the NVM is then read out again).

8.17 'Option number'

In case the EAROM has to be replaced, all the options will also require resetting. To be certain that the factory settings are reproduced exactly, both option numbers have to be set. These numbers can be found on a sticker on the picture tube.

Menu name	Subjects	Options	Physically in the set
	Video DualScreen	Yes No	Video DualScreen panel present (diagram AC) Video DualScreen panel not present (diagram AC)
Source Selection	SS Type	Euro MD2	Always in MD2
	Euro AV3	Yes No	3rd EURO connector present (diagram K) No 3rd EURO connector present (diagram K)
Audio Repro	Audio Repro	Basic Incr. sound Dolby + eq.	No dolby, no incredible sound, no graphic equalizer (Audio Module no dolby, no incr; diagram O) No dolby, yes incredible sound, no graphic equalizer (Audio Module no dolby with incred; diagram O) Dolby and so also graphic equalizer (Dolby Audio Module; diagram P / P2)
	Cordless Dolby	Yes No	Cordless dolby transmitter module present (diagram AE) Cordless dolby transmitter module not present (diagram AE)
	Dolby Signalling	Yes No	Automatic switching to dolby controlled by broadcaster is present (only software) Automatic switching to dolby controlled by broadcaster is not present (only software)
Miscellaneous	El. Program Guide	Yes No	IC7204 (flash memory) present on TXT+control module (diagram J) IC7204 (flash memory) not present on TXT+control module (diagram J)
	VGA	Yes No	VGA module present (diagram AF) VGA module not present (diagram AF)
	Telephone link	Yes No	Telephone interface panel present (diagram AJ) Telephone interface panel not present (diagram AJ)
	Heatsink Present	Yes No	Heatsinks present on CRT+scavem panel (diagram E) Heatsinks not present on CRT+scavem panel (diagram E)
	Philips logo	Yes No	Philips logo in Virgin mode and Demo mode (only software) No philips logo in Virgin mode and Demo mode (only software)

- If an option selection in the Service Alignment Mode is displayed in black letters, then that is the result of a different option selection in the Service Alignment Mode.
- After the option(s) have been changed, they can be stored via the STORE command.
- The new option is only active after the TV is switched off and then back on again using the mains switch (the NVM is then read out again).

8.16.2 Options in the Dealer Mode

Menu name	Subjects	Options	Physically in the set
Picture	Sharpness in menu	Yes No	Sharpness in picture menu Sharpness not in picture menu
	Tint in menu	Yes No	Tint (normal warm cool) in picture menu Tint (normal warm cool) not in picture menu
	CTI	Yes No	CTI enabled CTI disabled
	Subtitle Squeeze	Yes No	Subtitle squeeze enabled (moves subtitles upwards in case they would fall of the screen) Subtitle squeeze disabled
	Digital Options	100 Hz Digital Scan Natural Motion Nat. Motion Demo Split Screen	Only 100Hz is possible Only 100Hz and Digital scan is possible 100Hz and Digital scan and Natural motion is possible Demo mode; active areas are coloured in a black and white picture Demo mode; lower part is digital scan + natural motion / upper part is only digital scan

Ciruit description

9.1.4 Through-starting via self-oscillation (from the 2nd 50Hz cycle up to take over by the control loop) (Fig. 9.2)

Self-oscillation takes place as long as the secondary voltages are still not too low in order to allow the control circuit to work (so that it can still not be adjusted back).

- Immediately after starting up a linear increasing current flows through primary winding 5-1 which can never be higher than hfe x Ib.
- At the moment that this point is reached the primary winding 5-1 will hold its voltage as a result of which the impedance of the primary coil will start to drop. As a result of this the voltage over primary winding 5-1 and over the positive feedback winding 8-7 drops. The positive feedback current, the base and, as a result of this, the collector current of switching transistor TS7302 also drop, resulting in this starting to reverse.
  As a result of this pin 8 of the positive feedback winding becomes negative. The base voltage of TS7302 drops, the collector voltage increases, the positive feedback winding and the base voltage become more negative as a result of which TS7302 reverses more quickly (once again an avalanche effect, but now in reverse).
- Now that TS7302 is reversed, all energy which was stored in the transformer is supplied to the load.
  Because the secondary flows want to and can continue to flow (secondary diodes are conducting), the voltages reverse over the secondary windings and as a result of this the voltages over the primary windings also reverse.
  As a result of this the capacity on pin 5 of the transformer can charge up C2305 to the peak value of 900V (300V + (Vsec x n)).
- At the moment that all energy has been transferred from the transformer to the load, a resonance takes place between the primary winding 5-1 and C2305.
- If, during the resonance, the voltage over the primary winding 5-1 becomes positive, the voltage on the positive feedback winding 8-7 will also become positive. As a result of this the switching transistor will again start to conduct. This results in the voltage on the positive feedback winding 8-7 becoming high and the switching transistor again starts to conduct.
- This process repeats itself as a result of which the secondary voltages are built up more and more until the control loop, which provides the stabilization of the SOPS, comes into operation (see pulse width controller).

N.B.:

- Self-oscillation can also take place if the control circuit is faulty.
- Disconnecting pin 5 of the opto-coupler IC7301 and then carefully increasing the mains voltage using the VARIAC can be handy for fault tracing. As a result of this the SOPS is forced to continue running in self-oscillating mode.

9.1.5 Building up and maintaining the -5V on pin 7 of the transformer (continuous process) (Fig. 9.2)

In order to be able to quickly switch off switching transistor TS7302 and thus avoid its dissipation, -5V is applied to the base of TS7302 when switching off. The stabilization of pin 7 of the transformer is explained here.

- When switching transistor TS7302 is conducting, pin 8 of the transformer has +12V. Because *68328 and D6327 now* start to conduct, energy can be passed on from the source to the load. The output voltage over R3305 is stabilized exactly at -5V by the Zener -(5V6-0V6) via the 5V6 Zener and D6328 and the 0V6 of the BE of TS7300. R3343 and R3337 limit the current through transistor TS7300.
- During the reversal of switching transistor TS7302 the voltage on pin 8 of the transformer drops to -36V. D6327 and D6326 reverse and energy is no longer delivered to the load.

9.1.6 Stopping switching transistor TS7302 from conducting (Fig. 9.3)

The amount of energy which has to be pumped into the transformer has to be determined by the amount of energy which the load requires. In order to control this the pulse width controller on the secondary side makes the photo-diode in the opto-coupler conduct at just the right moment, as a result of which the switching transistor is ultimately reversed. This works as follows:
If the photo-diode on the secondary side starts to conduct, the photo-transistor on the primary side of the opto-coupler also conducts. As a result of this TS7310 starts to conduct, causing TS7311 to conduct. As a result of this the base of switching transistor TS7302 becomes connected to -5V via L5302 and R3306. A short and simultaneously very strong negative base current then flows as a result of which TS7302 reverses quickly and dissipates as little as possible. The quick 'drawing empty' of a transistor with a negative base current is called 'hollowing'.
During the reversal of switching transformer TS7302 there is a positive pulse on pin 5 and, due to this, also on pin 9 of the transformer. During this positive pulse TS7304 conducts as a result of which it is ensured that TS7310 and thus TS7311 also remain conducting. As a result of this TS7302 definitely remains in reverse when the high voltage is present on its collector.
Diodes D6305 and D6333 serve to protect transistors TS7304 and the opto-coupler.

9.1.7 Pulse width controller (Fig. 9.3)

Switching transistor reversed, energy to the load
As long as switching transistor TS7302 is reversed there is a negative pulse on pin 12 and pin 14 of the transformer.
The negative pulse on pin 14 charges C2312 negatively via D6315 and R3317 *(negative charging current I_A)*. As a result of this TS7305 reverses and no current flows through the diode of the opto-coupler. The secondary windings now deliver energy to the load.

Switching transistor conducts, energy in the transformer
As soon as all energy has been passed from the transformer to the load (secondary flow then becomes zero) the polarity of the voltages on the transformer reverses (see self-oscillation). Switching transistor TS7302 now starts to conduct and on pins 12 and 14 of the transformer there is now a positive voltage and on pin 22 a constant negative voltage.

Two current routes are created:
- Because pin 12 of the transformer is positive, D6313 and D6314 conduct and C2312 is charged up positively from its negative voltage (*positive charging current I_B*).
- The +16V output voltage is measured directly via TS7303. Because the voltage on pin 22 is now negative D6318 does not conduct as a result of which the base of TS7303 forms a direct reflection of the +16V output voltage via R3310, R3311 and R3312. For example, with an increase of the +16V the base will increase less than the emitter of TS7303, as a result of which TS7303 conducts more and thus generates a larger current (*positive charging current I_C*). Therefore, using R3311 the output voltage can be adjusted to +16V (so long as the switching transistor TS7302 reverses, pin 22 of the transformer is positive, D6318 conducts and the base of TS7303 lifts. Therefore this control only works as long as switching transistor TS7303 is conducting).

These two positive charging currents charge C2312 positively. As soon as the voltage on the base of TS7305 becomes higher than 1V2 TS7305, starts to conduct. The diodes and, due to these, the photo-transistor of the opto-coupler, conduct, as a result of which switching transistor TS7302 starts to reverse.

Load increase
With increasing load, the +17V and the -17V drop:
- Because the +17V wants to drop the base of TS7303 will want to drop by approximately half with regard to the drop of the emitter of TS7303. As a result of this TS7303 is driven less open, resulting in the *positive charging current I_C* decreasing.
- Because the negative pulse of pin 14 decreases when the output voltages are dropping, the *negative charging current I_A* will also decrease. However, due to the TS7303 control the power supply is correct immediately, as a result of which more energy is pumped into the transformer. As a result of this pin 14 again becomes more negative, causing the *negative charging current I_A* to increase again.
- The *positive charging current I_B* will remain constant because that is only related to the level of the primary voltage 300V (see mains voltage variations).

Due to the increased negative charging current I_A, C2312 becomes charged up more negatively and due to the decreased positive charging current I_C, C2312 will be charged up less quickly. Due to these two mechanisms it takes longer before C2312 reaches the 1V2, as a result of which TS7305 is switched later. As a result of this the switching transistor is switched off later and more energy is pumped into the transformer. As a result of this the load increase is compensated.

Mains voltage variations
When the mains voltage becomes lower, the positive voltage on pin 12 also becomes lower (thus lower than 10V). As a result of this the positive charging current I_B becomes smaller, as a result of which it takes longer before C2312 reaches the 1V2.

When the mains voltage becomes higher, the positive voltage on pin 12 becomes higher as a result of which C2312 charges up more quickly. As a result of this the duty-cycle reduces (T-on becomes shorter if T-off remains the same). In order to limit this duty-cycle when the mains voltage becomes too high the current path I_B receives and additional current path via Zener diode D6321 when the input voltage is too high. In this way there is an additional charge on C2312, as a result of which this charges up more quickly and the switching transistor switches off more quickly. The maximum duty-cycle is limited in this way so that the maximum power in the event of over-voltage can not then become greater than for nominal voltage.

9.1.8 Standby (Fig. 9.3)

If the set is switched to standby the 'St-By-INFO' is set low by the standby-µP (active low). As a result of this TS7312 reverses in standby, as a result of which TS7306 conducts via the +5STANDBY supply voltage, R3341 and D6317. Therefore, the diode of the opto-coupler conducts continuously in standby and the 'Audio power Supply' is completely adjusted back to 0V output voltage. In standby the photo-diode continues to be supplied by the +5STANDBY via D6316.

9.1.9 Protections (Fig. 9.3)

When a fault is detected on the 4 x 15W sound power amplifier panel, for example because the +16V or the -16V is too low or too high), this panel makes the 'DC PROT' line high (+5V). As a result of this TS7306 will conduct and adjust the power supply completely back (same principle as in standby).
D6316 ensures at the same time that switching transistor TS7302 does not become faulty if the positive voltage is not present on pin 12. The photo-diode is then supplied with the +5STANDBY.
As long as the +17V is greater than 19V4 then, via D6311, R3318, D6331 and D6308, transistor TS7306 will conduct and the power supply will be adjusted back to 0V.

9.2 Changes to the power supply section of the large signal panel

9.2.1 Semi-standby mode

For the main supply on the large signal panel it is the intention that in certain conditions the set can be placed in the semi-standby mode, for example as in EPG mode. This means that the power supply works completely but that the series switch is switched off so that the line stage does not operate. The switching on or off of the series switch takes place from the SSP panel via the 'SLOW DOWN' line. This semi-standby principle existed already in MD2.1 (i.e. when starting up the set the series switch must initially be open), but for MD2.2 there are a number of changes which have been made in the power supply section.

	TS7302 conducts, therefore energy into the transformer	**TS7302 reverses, thus energy to the load**	
C2312	positive charging current	negative charging current	
I_A as a result of U_{sec}	0	present	U_{sec} I_A C2312 charged up less negatively
I_B as a result of U_{prim}	present	0	U_{prim} , I_B , C2312 charged up positively more quickly
I_C as a result of U_{sec}	present	0	U_{sec} I_C C2312 charged up positively less quickly

Ciruit description

9.2.2 Degaussing circuit (only for EPG)

Principle
When changing over from standby to semi-standby in the EPG mode then the degaussing will not work correctly because people can be frightened by unexpected degaussing. To avoid this the degaussing may only take place if the mains voltage is switched off completely and then back on again. For this purpose the control of TS7507 is adapted for sets with EPG.

Operation
When switching on the degaussing switch, TS7505 is triggered via winding 5-6 of the transformer L5550 and TS7515 so that the degaussing can start. C2514 changes up via R3532. When, after this, C2514 is sufficiently charged up (this is determined by D6514), TS7513 and, as a result of this TS7514, will start to conduct. Once TS7514 is fully conducting, TS7512 will continue to conduct and, as a result of this, TS7514 will again continue to conduct (TS7512 and TS7514 together form a thyristor function) until the mains voltage is completely switched off.
Because TS7512 now remains conducting, the base of TS7515 remains high so that this continues to be reversed, with the result that TS7507 remains switched off until the mains voltage is completely switched off.
The number of windings on the transformer is increased so that even in standby the 'thyristor' TS7512-TS7514 remains operational. As a result of this, switching the degaussing back on is only possible after C2514 is sufficiently charged up, in other words after switching off the set.

9.2.3 Changes to the primary side for reduced standby power (only for MC44604) (Fig. 9.4)

Introduction
In order to reduce the dissipated power in standby (without degaussing) (< 2W) a new control IC has been selected, namely the MC44604 instead of the MC44603 (the power supply with the MC44603 consumed 3.75W in standby). This new IC has an integrated 'optimalized standby function'.

Higher burst frequency (the number of burst periods per unit of time)
In order to reduce the dissipated standby power the under-voltage level of IC7520 is increased only in the standby mode, as a result of which the burst frequency (the number of burst periods per unit of time) is increased.
This is done as follows:
In standby the Vcc of IC7520 increases via R3528 to the level Vth. As soon as Vth is reached the IC starts operating and generates control pulses. The power supply will now start up. Because the start-up circuit is unable to deliver sufficient current, the Vcc is normally taken over by the take-over winding 9-8 of the transformer. However, in stand-by mode the power supply is adjusted back so much that the take over is insufficient and the Vcc sinks immediately. As soon as the Vcc arrives below the under-voltage level the IC, and thus the power supply, will be switched off again and the Vcc will increase via R3528. Because with the MC44604 the under-voltage level is increased only in the standby mode, the number of burst periods is increased per unit of time. The frequency at which the power supply tries to start up during the burst is the same as that of the MC44603 and the same as that in normal operation (the power supply is an FFS (Fixed frequency Supply), in other words it also runs at approximately 40 kHz in standby mode).

Other changes to the primary side for reduced standby power for the MC44604
- R3528 is increased for the MC44604 as a result of which the dissipation in this resistor is smaller. In order to ensure that the start-up time is the same as before the C2525 is smaller for the MC44604.
- Because the C2533 (voltage on pin 11 determines the duty-cycle) is smaller for the MC44604, the duty-cycle is built up more quickly as a result of which the slow-start runs more quickly. As a result of this the burst period (the time that the power supply tries to start up in standby) is shorter, as a result of which the power supply itself works more efficiently (less dissipation losses in the power supply itself).

9.2.4 Changes to the secondary side for the reduced standby power (only for MC44604) (Fig. 9.5)

Place MC44604 in standby mode
The MC44604 must receive a sign in order to enter the standby mode with reduced burst frequency. Pin 15 of IC7520 is used for this. As soon as the input current on pin 15 is greater than 35 mA then IC activates its standby mode.
In order to create this current surge a change has been made to the secondary side of the main power supply. When the STANDBY signal is low (active), TS7589 will reverse as a result of which the full +5STANDBY power supply suddenly arrives on the positive side of C2590. C2590 is unable to follow this rapid change and drives TS7588 into full conductance as a result of which a large, brief current starts to flow through the photo-diode of TS7556 (opto-coupler). As a result of this a brief, strong current peak which flows to pin 15 of IC 7520, is generated on the primary side and the MC44604 activates its standby mode.

Maintaining power supply in standby mode for a power supply with the MC44604
Because C2590 charges itself up as soon as the standby mode is activated, at a given moment TS7588 will start to reverse. Because TS7591 only conducts continuously in standby mode (only in the standby mode is the +5STANDBY power supply on the base of TS7591 via R3586 and R3598), a current can only still flow through the diode of the opto-coupler via D6592 and TS7591 to earth. This current is large enough to maintain the standby state. Because TS7591 also conducts during the 'burst' (the time that the power supply tries to start up in standby) the power supply is adjusted back even harder during the 'burst'. As a result of this the 'burst' will not last as long.

Stable +5STANDBY with the MC44604
In order to prevent that the +5STANDBY becomes too low in standby mode as soon as the input voltage of the voltage stabilizer IC7560 is at the lowest point (as a result of which even a POR could be generated), a few changes have been implemented for the power supply with the MC44604:
- Due to the higher burst frequency the ripple on the 5STANDBY is smaller. As a result of this the smoothing capacitor C2571 can be smaller.
- D6561 has been replaced by a type with a low forward voltage (0V2), as a result of which less voltage loss occurs.
- The transformer has been examined again in order to obtain improved efficiency in standby mode.

In this way it is ensured that the input voltage of the voltage stabilizer IC7560 is always large enough to create the +5STANDBY.

Changes for normal operation with the MC44604

- D6550 is added to protect the power supply if the +5STANDBY fails. If the +5STANDBY fails, the STAND-BY signal drops out as a result of which TS7592 starts to reverse. As a result of this thyristor TH7590 starts to conduct as a result of which the voltage over C2561 and C2571 will become too high. Zener D6550 has been added in order to protect these capacitors. At the same time this Zener ensures that the power supply is adjusted back to its maximum. The power supply will start up again, be adjusted by the maximum again, etc.→ hick-up mode.
- Because more energy is demanded from the +8V6 power supply in the MD2.2, the +8V6 voltage stabilizer IC7569 is a type which only requires low over-voltage in order to be able to generate a stable +8V6 (a so-called 'low drop' type).

9.2.5 Primary over-voltage for the MC44604 (Fig. 9.4)

Over-voltage detection for the MC44604
For the MC44603, over-voltage detection takes place via the Vcc input of the IC. In the MD2.2 for an MC44604 the separate OVP input is used on pin 6 of the IC. Since the Vcc depends too much on the mains voltage (+300V DC) and the load, it is possible that at high load large peaks arrive on Vcc as a result of which the OVP is triggered. Therefore, the voltage on winding 9-8 of the transformer is detected via a clamp circuit and a divider (D6548, R3548 and R3549). Only if pin 6 becomes higher than 2V5 will the power supply go into protection (hick-up mode).

Operation at increased input voltage (+300V DC)
In order to obtain a more constant output power as a function of the mains voltage, R3529 is added between the +330V DC and the current sense pin 7 of the IC. This sets a DC component which is dependent on the level of the +300V DC on the current sense input at the top of the current sense voltage, such as that which is measured on the source of the TS7541 FET-link. As soon as the +300V DC increases the complete current sense signal is raised a little on pin 7 as a result of which the T-on decreases by a constant value.

Video processing

9.3 PALplus (fig. 9.6)

9.3.1 Introduction

With 16/9 sets, the PALplus module takes care of both the vertical conversion and also the improved separation between luminance and chrominance.
The module receives the 8 bit Y, 2 bit U and 2 bit V signals from the A/D convertor in the Feature Box. After the PALplus decoding, the signals again go via the AI panel to the Feature Box, where the 50 Hz picture is converted to 100 Hz. Control is provided by the *snertbus* of the processor on the Feature Box. The PALplus module, the AI PCB and the Feature Box are connected by a series of timing signals.

9.3.2 General operation

The MACPACIC (Motion Adaption Colour Plus And Control IC) is controlled by the *snertbus*. The most important
function of this IC is to take care of the separation between luminance and chrominance if MACP is used in the transmitter. The MACPACIC uses both the direct Y, U and V and also those stored in MEM1.
MEM4 is an extra working memory.
The processed picture information is written to memories MEM2 and MEM3.
The VERIC (Vertical Reconstruction IC) reads Y, U and V from memories MEM2 and MEM3 and once again makes a picture of 574 lines from the 430 picture lines by means of the 144 helper lines. This IC is monitored by the MACPACIC which generates a number of clock and sync signals for this.
The module input and output are 16 MHz. The module operates at 32 MHz.

9.3.3 Motion Adapter Colour Plus

The MACPACIC sees to separation of chrominance and luminance if MACP (Motion Adaption Colour Plus) is used in the transmitter. Because of this, the picture is free from chrominance and luminance crosstalk.
The first raster is written to memory MEM1. When the second raster is presented directly to the MACPACIC, MEM1 will be read out causing both rasters to be present at the same time at the MACPACIC input.
MACP can be used independently of the picture mode, i.e. also with 4/3 transmissions.

9.3.3.1 Film mode
In the film mode, 50 rasters are made of the 25 pictures in the transmitter. There is no time difference between the successive even and odd rasters. Because of this,
the picture information of line N in the even raster will be nearly identical to that of line N in the following odd raster. The chrominance of line N in the first raster is in phase opposition to the chrominance of line N+312 in the second raster. In the receiver, addition of the even and odd rasters will thus produce a Y signal which is free from chrominance. Because of this, no further suppressions of the chrominance
at 4.43 MHz are required in the Y channel.
After the PAL demodulator, frequencies around the 4.43 MHz in the Y signal give a U and V component which is in phase opposition for the lines N and N+312. Addition of two successive rasters in the U and in the V channels will eliminate this colour component.
These operations are termed FCP (Fixed Colour Plus), which produces the same result as a comb filter.

9.3.3.2 Camera mode
In the camera mode, unlike the film mode, there is a time difference between the successive even and odd rasters. This time difference causes differences in the successive rasters, especially in content, with fast-moving pictures. The aim will always be to switch over to FCP as far as possible since this gives the best picture quality. This is only possible however if there is almost no difference in picture information with the successive rasters.
Accordingly a movement detector is built into the decoder and this determines for each small part of the picture whether any movement is present. Memory MEM4 is used for this.
With pictures where there is little movement, indicated by the movement detector, switchover to FCP occurs.

With fast-moving pictures the bandwidth of the Y signal is limited to 3 MHz, because of which the chrominance is removed at 4.43 MHz. The resulting Y, U and V are written by the MACPACIC to memories MEM2 and MEM3.

9.3.4 Vertical conversion

To reproduce a 16/9 picture in a 4/3 format the 574 picture lines are converted to 430 lines in the transmitter. Because of this, picture information is lost, and without correction this leads to reduction in the vertical resolution.
To be able to make good this loss in vertical resolution, the 'lost' Y information is AM modulated on a 4.43 MHz carrier wave with the same phase as the U signal and is processed in the black bars above and below the picture.
The 72 lines in the black bar above the picture contain the 'lost' information of the upper half of the picture. The 'lost' information from the lower half of the picture is to be found in the 72 lines in the black bar below the picture. These lines with modulated 'lost' information are also termed 'helper lines'.
The VERIC will once again make a picture of 574 lines from the 430 picture lines.
A 'reconstruction' takes place for the Y signal, in which use is made of the 144 helper lines. Since no helper signal is present for U and V, these are determined by 'interpolation'.
When the upper half of the picture is processed, the helper lines are routed to MEM2 and the picture to MEM3. For the processing of the lower half of the picture, the picture goes to MEM2 and the helper lines to MEM3.
Writing to these memories is done by the MACPACIC, readout being carried out by the VERIC.
In film mode, a complete picture is present after two rasters and because of this the conversion will take place for each picture.
In camera mode because of the time difference between two successive rasters there is a difference in picture content because of which conversion must be carried out for each raster. The helper lines are then composed differently and the use of the memory will therefore also be different.

9.3.5 Transparent mode

With a non-PALplus transmission, luminance and chrominance are switched through in the MACPACIC.
The top and bottom picture halves are routed respectively into memories 2 and 3. The VERIC then sees to it that the information for the even and odd raster is read in the correct way.

9.3.6 Detection

To be able to recognise when this extra PALplus information is present in the video signal and to be able to detect and demodulate this correctly, some extra information is also added.

Line 23 therefore contains no picture information but does contain some signalling bits such as:
- camera or film mode
- MACP used
- helper lines present.

These bits are detected by the MACPACIC.
This line also contains a reference burst with the correct amplitude, DC and phase for the helper lines.
Line 623 contains the reference level for white and black.

9.3.7 Remarks

With a PALplus set, the chrominance IC TDA9144 is used instead of TDA9141 or TDA9143.
The helper lines with Y information modulated at 4.43 MHz, are demodulated in the PAL demodulator and multiplexed in the Y signal. Since information which comes out below the back level is present here, the blanking in the IC has been adjusted.
The chrominance IC TDA9144 generates line 22 which contains the references for the black level and the DC level of the helper lines. Some filters in the IC, both in the luminance and in the chrominance channel, are if necessary switched off with PALplus.
There is no PALplus recognition within the TDA 9144. This means that all PALplus functions from the microprocessor must be indicated via I²C.
The microprocessor in turn receives PALplus recognition information from the PALplus module.
The MACPACIC generates the 16 MHz and the 32 MHz clocks. The phase between these two clock signals is adjusted by S5100.
All processing operations in the PALplus module are digital.

9.4 CRT & Scavem

9.4.1 Power limiting of the RGB amplifiers

9.4.1.1 Introduction

The RGB output amplifiers are identical to those used in the MD 2.1, though in the lowest segment of the MD2.2, the RGB output stages are no longer fitted with heat sinks. To ensure that the dissipated power, which is produced chiefly at high frequencies, remains within the limits of these output stages, an extra circuit is added. In case of consumption greater than 3.6 W (measured via R3373), this circuit will reduce the definition of the picture. This causes the current consumption of the output stages to fall. In practice, this power reduction circuit will only be activated in case of a picture with a great deal of noise.

9.4.1.2 Circuit

The power consumed by the output ICs is detected across resistor R3373; this is fed to TS7374. This is an amplifier with an amplification factor of -1.
The collector voltage of TS7374 is thus equal to the voltage measured across R3373.
If the collector voltage of TS7374 rises, then TS7377 will conduct more and the collector voltage of TS7377 falls.
In case of current consumption higher than 18 mA (3.6 W), the collector voltage of TS7374 becomes greater than 6 V, the collector voltage of TS7377 becomes lower than 11.4 V and because of this, TS7338, TS7348 and TS7358 start to conduct.
When these transistors conduct, a capacitance is placed in parallel with the input signal, causing the picture definition to be reduced and the current consumption, and thus the dissipation too, to fall once again.

9.4.2 Improved SCAVEM

To improve Scavem operation, a larger current of about 1 A pp is sent through the Scavem coil. To achieve this, the amplification of the output stage is adjusted (R3408 200 ohms instead of 100 ohms) and the output transistors TS7414 and TS7415 are changed to power transistors (BD139, BD140).

Ciruit description

9.5 Luminance Transient Processor (LTP) (fig. 9.7)

9.5.1 Introduction

In the MD2.2, the LTP IC TDA9177 may optionally be added in front of the video control IC TDA4780. This IC is I²C controlled and carries out some corrections to the Y signal. These are:

- smart peaking
- step improvement
- noise suppression

9.5.2 Functional description

9.5.2.1 The input signals

The input signals are formed by YUV on pins 5, 9, 7 and a sandcastle on pin 1. The output signals are YUV on pins 20, 16 and 18. The U and V signals are delayed according to the corrections to the Y signal.

9.5.2.2 Smart peaking

Smart peaking is a circuit which only applies peaking to small signal changes; because of this, details in the picture can be seen more clearly. The extent of peaking and the signal amplitude to which smart peaking operates, can be adjusted via I²C. With large signal amplitudes (e.g. with black-white transitions) there will be less peaking to avoid unwanted shadow effects. When the LTP is used, the software peaking of the Feature Box will be turned off but the hardware amplification continues to operate.

9.5.2.3 Step improvement

This provision ensures than black-white transitions are made even steeper. The result of this is that the picture gives a still sharper impression.

9.5.2.4 Noise suppression

The LIMERIC in the Feature Box determines the noise level in the picture and appraises this by means of the noise figure which is passed on via I²C to the microprocessor. On the basis of the noise figure, in addition to the degree of noise suppression in the LIMERIC and the degree of DNR, the degree of peaking together with the 'steepness' and the 'coring' in the LTP is now also reduced in proportion with the rise in the noise figure. Because of this, even better noise suppression can be arranged.

9.6 Chrominance notch filter

As well as a chrominance-free Y signal, the COMB filter also produces a few unwanted residues in the vicinity of 4.43 MHz. These residues can be clearly seen when there are sharp colour transitions. To suppress this interference, a filter is fitted between the Y output of the COMB filter and the input of the chrominance IC (IC 7352). This filter is switched on together with the COMB filter. As soon as the COMB filter is switched on (COMB ON/OFF is high), TS7396 will then conduct and the LC circuit (C2351, C2352 and L5382) is switched on. This LC circuit gives an extra 6 dB of suppression at 4.43 MHz.

9.7 Transparent OSDs and menus (fig. 9.8)

9.7.1 Introduction

In the first instance, the operating menus of GFL and MD2.1 consisted of a menu block with a background colour and printed on it the menu text in a foreground colour. With the menus of the MD2.2, the menu block with background colour is replaced by a block in which the main picture is displayed attenuated and the menu text is shown in white on it. With the so-called 'Blending' circuit it is possible to display these so-called 'transparent operating menus' on the screen.
To produce these menus, a number of control signals are required, such as the RGB signals and the Fast Blanking. These four signals were hitherto sufficient to be able to display a menu. However, for the transparent operating menus an extra timing signal is required, namely the COR-NOT signal. The signals are now used as follows:

- At the time that the 'menu block' is written, the TXT-IC produces a low on the COR-NOT line. At that time the blending circuit will ensure that if a specified beam current is exceeded, the contrast is reduced via the beam current limitation in the video controller TDA4780. By only reducing the contrast with effect from a specified beam current, darker picture sequences are displayed unaffected so as to prevent these disappearing completely below the black level.
- However, when text is to be displayed in a menu block, the Fast Blanking information is used to switch off the blending circuit again. Because of this, the contrast is not reduced only where the text is shown in white.

9.7.2 Blending circuit

The blending circuit is located on the TXT+control panel.
If we assume in the first instance that there is no menu (COR-NOT line is high), then TS7453 conducts and TS7454 is in the blocking state. Because of this, TS7455 conducts in such a way that TS7457 blocks sufficiently to ensure that the V_{OUT} can follow the V_{BCI} via the BE of TS7459 and the BE of TS7458. At the time the menu appears, the COR-NOT line will become low and TS7454 will conduct. The resistor division R3445 and R3443 now sees to it that the base of TS7455 is set to 2V8.

- As long as V_{BCI} < 2V8, V_{OUT} follows the V_{BCI} via the BE of TS7459 and the BE of TS7458. This applies to the darker picture sequences and so these are not attenuated.
- If a voltage increase to above 2.8 V occurs, the base of TS7455 will only partially rise (due to the voltage division R3443, R3444, R3445). This only partial voltage rise is passed through the BE of TS7455 and the BE of TS7457 to the V_{OUT}. Because of this, the V_{OUT} will rise less strongly only if the V_{BCI} is greater than 2V8 (lighter picture sequences). This results in a reduction in contrast.

In other words, the DC setting of the base of TS7457 governs the changeover point of the contrast reduction (and thus the brightness at which the contrast reduction must begin with transparent menus).

9.7.3 PIP in front of TXT in a set with blending circuit

In a set without transparent OSDs and menus (MD2.1), it is desirable to have the PIP card always in the foreground (and thus in front of the menus, in front of the OSDs and in front of the TXT). This is done in MD2.1 via the TXT-KILL line and TS7518 (in PIP-mode TXT-KILL is high causing the FBL-TXT to be short-circuited (deactivated) via TS7518).
In a set with transparent OSDs and menus (MD2.2), the PIP card is placed in the background so that the PIP card is viewed through the transparent OSDs and manus. Only in the TXT mode is it desirable to have the PIP card in the foreground. For this the circuit round TS7221 has been added to the FBL-TXT line on the TXT+control panel. C2220 is chosen so that TS7221 passes the FBL-TXT signal to the TXT-ENABLE only in the TXT mode and not in any other modes.

- Only in the TXT mode is the FBL-TXT line constantly high so that C2220 is charged and TS7221 conducts constantly. The FBL-TXT is passed to the TXT-ENABLE and therefore with PIP the FBL-TXT is short-circuited via the TXT-KILL (PIP in front of TXT).
- In all other modes (e.g. OSDs, menus and TXT-mixed mode), FBL-TXT is not constantly high. Because of this, C2220 is not sufficiently charged so that TS7221 is constantly in the blocking state. Because of this, the FBL-TXT is not passed to the TXT-ENABLE so that with PIP, the FBL-TXT cannot be short-circuited via the TEXT-KILL (PIP behind OSDs, menus, mixed mode).

9.8 Automatic Aspect Ratio Adaption (AARA)

9.8.1 Introduction

With certain wide picture transmissions, the WSS bit (Wide Screen Signalling bit) is not included with the transmission. This applies to transmissions in 22/9, 16/9 or 14/9 format.
The customer on the reception side is then faced with a picture where the format is not correctly adjusted (black bars). This can then only be corrected by operating the picture format button on the remote control.
AARA now provides automatic adjustment of the picture format.

9.8.2 Operation

The software in the Feature Box contains a 'black bar detection algorithm'. This black bar detection looks to see whether black bars are present at the top or bottom of the picture. This is done by means of the SMARTIC.
If these bars are present for more than 22 seconds then the picture format is corrected to a maximum of 22/9. The picture width is adjusted by the PANIC and the picture height by the PROZONIC/MELZONIC.
Black bar detection operates independently of the operating software of the set.
Black bar detection can be overruled by:

- the WSS bit
- by an external 16/9 status on a scart input
- by adjusting the picture proportions manually

This function is implemented independently by the software in the Feature Box.

Audio processing

9.9 Audio amplifier

9.9.1 Introduction

For the MD2.1 sets we had different versions:

- Non Dolby fighter version
- Non Dolby horn version
- Non Dolby subwoofer version
- Dolby subwoofer version

In order to be able to delivery more audio power, for the most expanded MD2.2 a choice can be made for a separate audio amplifier, the so-called Audio Amplifier module. For this the audio power supply has to be stronger, as a result of which a stronger power supply unit - the so-called 'Audio Power Supply' - is used. As a result of this we have one additional version in the top MD2.2 sets:

- Top Dolby subwoofer version 4 x 15W.

9.9.2 Block diagram of the Dolby subwoofer version (Fig. 9.6)

The audio signals Surround, Left, Right and Centre originate from the Dolby Audio Module. The power of the output amplifier is 15W per channel.
On the LSP the output amplifier in a Top Dolby subwoofer version is only used for amplifying the surround-sound signal. This has the advantage that a separate channel is provided for both L and the R surround. Because the output signal from the amplifiers is at a DC level of +14V, the outputs are AC coupled to the surround loudspeakers.
On the Audio Amplifier Panel the amplifiers are localized for the Left, Right, Centre and Subwoofer signal.

- The signal which is intended for the subwoofer is a mono signal (L and R are added), because the low frequencies are not direction sensitive. The higher frequencies are filtered out from 270 Hz. The DBE circuit which was previously on the LSP, has now been mounted on the Audio Amplifier Panel. This DBE (Dynamic Bass Enhancement) circuit provides an improvement in the low tone reproduction which is supplied to the subwoofer. The lower half of IC7740 is used for amplifying the subwoofer signal.
- The L and R signals are amplified in the 2 upper halves of amplifiers IC7740 and IC7750. The L and R signals both run via a 200 Hz filter to the internal squeeters which provide the stereo effect, or directly to the internal loudspeakers. In the latter case the input of the subwoofer amplifier is also connected to earth.
- The Centre signal runs via a high-pass filter at 310 Hz and the lower half of amplifier IC7750 to the centre speakers at the bottom centre of the set.

The internal or external selection is determined by a switch on the Clickfit Panel.

9.9.3 *Internal/external selection (Fig. 9.10)*

The selection is made using a switch on the Clickfit Panel which sends either +6V or earth to pins 9, 10 and 11 of IC7735.
For the internal mode pins 9 to 11 (inclusive) are set low. As a result of this all switches are in the lowest position.
For the L and R signal which is intended for the squeeters, all frequencies lower than 270 Hz are filtered out first.
Before these signals arrive on the output amplifiers they are initially attenuated by R3700, R3701, R3702 and R3703.
The power supply for these output amplifiers is symmetric (+16V and -16V), as a result of which all outputs can be coupled directly to the loudspeakers. The amplification is determined internally in the output amplifiers by means of 2 internal resistors between the input and the output.
The Boucherot filter consists of C2746, C2776 and R3746 and serves to filter out oscillations at high frequencies.
All amplifiers are almost identical, only the values of the Boucherot filter can vary depending on the type of loudspeaker which is used.
The subwoofer signal is a mono signal and runs via the DBE circuit to the respective output amplifier in the internal position.
In the internal position the subwoofer signal from the output amplifier is connected to earth, as a result of which the subwoofer is switched off. The L and the R signal is sent directly to the output amplifiers.
The centre channel remains operational, irrespective of the position of the INT/EXT switch.

9.9.4 *Mute circuit (Fig. 9.10)*

The sound can be muted in various ways in the output amplifiers:

- When the supply voltage becomes smaller than +6V or -6V, the IC will automatically interrupt its non-inverting input. This IC therefore automatically suppresses unwanted signals when switching on and switching off.
- The mute can also be activated externally (active low) via the AMP-MUTE2 line, which originates from the mP. This mute is switched off by the remote control, blue mute, programme switching, etc.
- When switching on the mains voltage, electrolytic capacitor 2788 forms a brief short-circuit, as a result of which the voltage is held low at point 2, as a result of which the IC is muted. This avoids a plop when switching on.

9.9.5 *Protecting the audio output stage (Fig. 9.10)*

The supply voltage of the output amplifiers is symmetrical (+16V and -16V). Therefore the outputs from the amplifiers are connected directly to the loudspeakers.
Therefore, during normal operation the output signal contains no DC components. C2761 can absorb any small fluctuations.
If one of the supply voltages now becomes too high or too low or if DC components arrive on one of the outputs because, for example, an IC is faulty, then TS7760 or TS7761 will start to conduct. As a result of this a current flows through R3760 which causes TS7762 to conduct.
The DC-PROT / STBY line therefore comes to 5V, as a result of which the Audio Power Supply goes into protection.
If the positive and the negative supply voltages reduce simultaneously, the voltage on C2761 remains at approximately 0V.
On the centre signal there is a DC voltage of approximately 6V, this is on the emitter of TS7767.
When the +16V becomes lower than 11V, TS7767 and thus TS7760 start to conduct and the DC-PROT signal will still be activated.
In stand-by the 16V supply voltage is switched off; the DC voltage on the centre signal is 0V and TS7767 does not conduct. The C AC signal is max. 0.5V and does not influence the circuit.

9.9.6 *DBE circuit*

DBE or 'Dynamic Bass Enhancement' is used in order to obtain an improved lower tone reproduction using the same subwoofer.

- Circuit 1 adds the L and R signals (the subwoofer requires the low information of both signals) and sends this added signal through a low-pass filter. All frequencies higher than 270 Hz are feedback intensely.
- Circuit 2 has a suppression at 70 Hz (90 Hz for Acoustic Horn).
- Circuit 3 has a frequency-dependent feedback. At 60 Hz the feedback resistance, and thus the amplification too is the greatest. D6720 and D6721 form a limiter if the signals one too large. Circuits 2 and 3 together form an amplification of the frequencies around 60 Hz.
- Circuit 4 is an invertor which 'rectifies' the signal again before it goes to the output amplifier of the subwoofer. By using this stage the amplification factor can still be changed if required. At the same time R3728 and C2728 form a filter which truncate all harmonics above 700 Hz which are caused by the DBE circuit.

9.10 Audio path on the Dolby Audio Module for Double Window (Fig. 9.11)

The 'Double Window' feature also has consequences on the audio section. For Double Window it applies that the sound of the main picture (the left picture) always goes to the loudspeakers, while the sound of the second picture (the right picture) goes to the main headphones.
The additional headphone selection takes place by using an additional switch SK4 and TDA9860.
SK4 provides the selection for the various audio sources, while TDA9860 makes the selection between:

- The classic headphones.
- Double Window headphones originating from an external audio source (SK4).
- The mono signal originating from the tuner on the Full Double Window module.

The configuration around SK1 is identical to that of MD2.1 with the difference that in the MD2.1 this switch was mounted on the SSP and all signals required in the MD2.2 are supplied to the Audio Module via a ribbon cable from the SSP, where the switch is now mounted.
Because SK1 is now on the Audio Module, SK4 can now be switched parallel directly here. This HEF provides the selection of the various audio sources for the headphones in Double Window. SK4 is driven by 2 bits of IC7590 which are applied via I^2C.
Both HEF's are supplied with an 8V5 power supply which comes from the SSP.
For SK1 there are two inputs for front: front L/R and front L/L. As a result of this it is possible to place a mono signal, originating from the front, onto both the left-hand and the right-hand channel.

However, SK4 has no automatic answer to both channels for the front input (all inputs are occupied), for a mono front signal only the left-hand loudspeaker will be driven to full power.
This is solved by IC7590. For a mono signal IC7590 places the mono signal on both the left-hand and the right-hand side. IC7590 is a TDA9860 which is also used in the GFL. However, for the MD2.2, 3 functions of the IC are used as additional functions with regard to the GFL (the remaining functions are 1 to 1 identical):

- The selector switch
- The volume control: which can now no longer be executed on MSP3410 because not all audio sources are offered to MSP3410 for the 'Video Dualscreen' headphones.
- The 2 control bits (pin 2, 31) for SK4.

Ultimately the input of IC7590 is sent to the headphones amplifier.

Wireless dolby

9.11 Transmitter (Fig. 9.12)

9.11.1 Block diagram

We can recognise 3 basic blocks in the block diagram of the transmitter:

1 FM transmitter (1403)
The FM transmitter is a screened module which is I^2C controlled by the main-μC of the TV:
   * At program switching the incoming surround sound signal from the Dolby Audio Module is muted (by the dolby IC SAA7710)) to avoid plops in the surround speakers.
   * At switching off the surround mode, first the incoming surround sound signal is muted (to avoid plops) and then the local oscillator in the transmitter is switched off. As the local oscillator is switched off also the 19 kHz pilot and the 433 MHz carrier are no longer be transmitted any more, which is recognised by the receiver. In that case after 15 seconds the receiver switches to standby.
   * Selection between the 7 channels around the 433 MHz.

2 Audio path
The basic audio path contains of plug 1409, input buffer IC7401A, a 15 kHz low pass filter L5401 (prevent high frequencies to the compander), a compander (IC7403 and IC7402B) and a buffer IC7404A.

3 Pilot generator
Although the transmitter transmits a mono signal, a pilot at 19 kHz pilot is used to enable the receiver to recognise whether the received signal is the wanted signal. This 19 kHz pilot is generated by an 38 kHz oscillator and a 2-divider around IC7404D/C.
Just before injection the pilot is added with the companded and buffered mono surround signal.

9.11.2 Compander

As the transmitter is an FM-transmitter, the amplitude of the audio and pilot signal is 'real time' converted into a FM-sweep. Large amplitudes are converted into a large FM-sweeps, small amplitudes into a small FM-sweeps. Small FM-sweeps have a bad signal to noise ratio and large FM-sweeps increase the required bandwidth. Therefore a so called 'compander' is used to limit the bandwidth and to increase the signal to noise ratio of the transmission. This compander attenuates large amplitudes (e.g. +10 dB to +5 dB), bypass middle amplitudes (0 dB to 0 dB) and boosts small amplitudes (e.g. -20 dB to -10 dB). On the receiver part this correction is corrected back by a so called 'expander'.
The basic compander configuration is given below. There is a variable gain cell (variable resistor inside NE572) in the feedback loop of an Op Amp (NJM). The resistance of the gain cell is controlled by the voltage across C2408 which is charged by the rectifier.

9.11.3 Pilot generation

The pilot oscillator is build around a 38 kHz tuning crystal 5403. Two inverters IC7404E and IC7404F - used as amplifiers - are used to make a buffered 38 kHz square wave signal.
The 38 kHz block is divided by 2 by the circuitry around the inverters IC7404D and IC7404C.

- On the moment the 38 kHz block becomes 'high', D6401 and TS7405 conduct. Via D6401 the input from IC7404D becomes 'high'. The output of IC7404D becomes 'low' and so the output of IC7404C becomes 'high' and keeps the input of IC7404D 'high'.
  As TS7405 conducts, C2438 is charged.
- On the moment the 38 kHz block becomes 'low', D6401 and TS7405 block. By now C2438 is discharged via R3449 as the input of IC7404C is still 'low'.
- On the moment the 38 kHz block becomes 'high' again, D6401 and TS7405 conduct. By now the input of IC7404D becomes 'low' as C2438 is still 'low' and TS7405 conduct. This 'low' on the input from IC7404D is long enough 'low' (via D6401 it wants to become 'high' again), to trigger the hold-circuitry IC7404D and IC7404C to a 'low' state.

The output is a sine wave due to the low pass filter R3450 and C2439. TS7406 is a buffer of the 18 kHz pilot generator.

9.11.4 Pilot and companded surround sound adding

The buffered and companded mono surround signal is fed to TS7410. This TS7410 has 3 functions:

- Adding the buffered and companded surround signal with the 19 kHz pilot.
- Buffer for the surround signal.
- Low-pass filter at 60 kHz via C2435.

Before injection into the modulator input there is the provision to align the maximum modulation (maximum FM sweep of 75 kHz) with potentiometer 3442.

9.12 Master and slave speaker box (Fig. 9.13)

9.12.1 General

The master and slave speaker box can be used wireless and wired. In case the system is used wired the cinch-plug on the master is used as input and the system automatically switches into the wired mode (by then as incoming signal from the TV the amplified surround signal from the rear speaker clickfit connector of the TV is used). Both wired and wireless make use of the amplifier in the master box. The slave box is a loudspeaker only which is driven by the master box. The following main circuitries are located inside the master box:

- Supply
- Receiver
- Amplifier

9.12.2 Supply

The supply consists of two conventional 50 Hz mains supplies.

- The standby supply is built up around mains transformer 5312. This standby supply starts immediately when the mains-switch TV-3 is switched on. By then via bridge rectifier D6312-6315 and stabiliser TS7275 the supply voltages V! and V2! are present.
- The main supply is built up around mains transformer 5313. This main supply is only active when the set is in normal operation and takes over the largest part of the energy delivery to stabiliser 7275 via D6260. In normal operation STBY_COM! is 'high', TS7273 blocks, TS7274 blocks, via R3316 TS7310 conducts and so relais 5310 is energized and the switch is closed.

Different situations:

- *Start up*
  At start up the system with mains switch TV-3, C2293 is charged but is even discharged faster via the 2 diodes D6278 and D6277. TS7272 blocks, TS7274 blocks, TS7310 conducts and so both supplies start up immediately.
- *Switch off*
  At switching off the system with mains switch TV-3, C2293 is not discharged any more via the 2 diodes D6278 and D6277. As a result C2293 is charged quickly and so immediately switches off the main supply. In this way a switch-off plop is prevented.
- *STBY_COM!*
  In case the STBY_COM! signal becomes 'low', the system must go into standby mode. In case STBY_COM! becomes 'low', TS7273 conduct, TS7274 conduct, TS7310 blocks and the main supply is switched off.
- If STBY_COM! is 'low' TS7265 will conduct and switch on the red LED. If STBY_COM is 'high', TS7265 blocks, TS7266 conducts and so the green LED is switched on.
  - ★ STBY_COM! 'low' → receiver in standby mode, main supply switched off, red LED
  - ★ STBY_COM! 'high' → receiver in normal operation, main supply switched on, green LED

9.12.3 Receiver

9.12.3.1 Block diagram

We can recognise 4 basic blocks in this diagram:

1 Frontend (1710):
Here the incoming 433 MHz aerial signal is filtered, amplified and via a mixer converted to a fixed 10.7 MHz IF frequency. The frontend is housed in a separate shielding unit to minimise the local oscillator radiation. There is an antenna connected to the input of the frontend.

2 IF and decoder part (7710):
Here the 10.7 MHz IF signal is filtered via 2 standard FM ceramic filters and fed to the IF FM-demodulator IC7710. In this IF FM-demodulator the mono surround signal is demodulated and the field strength and the presence of the pilot of the incoming 10.7 MHz signal is measured.

3 Audio path:
The received audio signal is filtered and expanded in dynamic range, to correct the companding circuitry at the transmitter side. This circuit uses the NE572 hi-performance circuit with an extra opamp. Basically this circuit multiples the incoming dynamic range with a factor of 2 dB.

4 Microcomputer (7750):
The μC reads the position of the 7-fold channel switch, controls the frontend via I²C and drives its mute pin.

9.12.3.2 IF demodulator

To make discrimination possible between the 7 channels that can be selected some selectivity has to made at the IF channel. Two standard 10.7 MHz ceramic filters with TS7707
in between are used for optimal behaviour towards S/N.
The IF-demodulator IC7710 (LA1805) has a main IF amplifier, and a FM and AM (not used) detector.
The IF-signal comes in at pin 1 and is boosted by a very high gain to a level where it is suitable for detection.
The detector needs a quadrature coil at pin 20.
The detected signal comes out at pin 17 and goes in again at pin 16. The stereodecoder is used for pilot detection only and is a classic system with a VCO (Voltage Controlled Oscillator) running at 152 kHz which can be adjusted by potentiometer 3721.
The AF outputs (pin 9 or/and 10) are filtered and amplified before they are presented to the expanding circuit. The filter 5730 is a double notch filter with filters out peaks at 19 and 38 kHz.

9.12.3.3 Expander circuit (IC7770)

The key IC is the NE572 which is used as an expander. Via this expander, the compander function in the transmitter side is corrected. This expander boost the high amplitudes (e.g. +5 dB to +10 dB), bypass middle amplitudes
(0 dB to 0 dB) and attenuates low amplitudes
(e.g. -10 dB to -20 dB).
The circuit is in fact a standard opamp (NJM) circuit where the input series resistor is formed by a gain cell. This gain cell is a variable resistor that is driven by a current that is obtained by rectifying the input current. Any variation of the cell impedance will change the gain of the main opamp NJM4560. Now the input of the gain cell and the rectifier are tied to the same level. When the input signal Vin drops by e.g. 6 dB, then the gain control current from the rectifier will also decrease with 6 dB (factor of 2).

Therefore the total change in Vout will be 12 dB, giving in fact a factor 2 (in dB) expansion. The detector circuit rectifies the input signal current. The V_{REF} for the opamp is extracted out of the NE572 IC via proper RC elements.

9.12.3.4 Microcomputer (IC7750)

The microcontroller is a MC68HC05 type with 1.2 kbit ROM and 14 I/O lines. The μC clock frequency is derived from a ceramic resonator of 4 MHz.
The internal clock is divided down to 500 kHz internally.
The reset circuitry around TS7755 creates a POR for the μC to assure that the μC only starts its program when the supply voltage is stable enough. The μC has the following functions:

- Read the setting of the 7 position slide switch continuously. In an internal look-up table the 7 required frequencies for the local oscillator are stored.
  The μC controls the local oscillator in the frontend 1710 to 1 of the 7 desired channels via the I²C bus. The output towards the synthesiser chip in the front-end is in I²C format, however there is no real handshaking as the synthesiser is the only device on the bus.
- In case the μC operates a channel switch, pin 11 is made 'high' for a moment. This to prevent plops when switching from one channel to another.
- In case the μC has detected that the receiver 1710 has received an incoming signal which is under the threshold level for more than 90 seconds, than pin 11 is made 'high' constantly.

9.12.3.5 MUTE signal

The MUTE signal on pin 5 of plug 1791 is 'high' in one of the following possibilities (OR-function):

- In case the 10.7 MHz field strength at the input of the IF-detector IC7710 is not strong enough. By then pin 8 of the IF-demodulator IC7710 and so - via D6710 - the MUTE signal becomes 'high'.
- In case the 19 kHz pilot-tone is not detected, pin 7 of the IF-detector IC7710 and so via D3710 the MUTE signal becomes 'high'. Even though the transmission is mono, this pilot tone is used and detected just to recognise that the received signal is the required signal.
- In case the μC operates a channel switch, pin 11 is made 'high' for a moment. This to prevent plops when switching from one channel to another.
- In case the μC has detected that the receiver 1710 has received an incoming signal which is under the threshold level for more than 90 seconds, than pin 11 is made 'high' constantly.

This MUTE signal is used for:

- Direct muting of the AUDIO signal at pin 2 of 1791 via mute circuitry TS7784 and TS7789. These transistors are connected inverse (collector and emitter are changed), but the functionality is the same. In case MUTE is high, the base-collector diode conducts and short the AUDIO signal via the emitter to the collector. In this way a better MUTE behaviour is obtained.
- Further this MUTE signal is fed to the circuitry which drives the STBY_COM! on the amplifier module.
  In case the MUTE signal is 'high' for more than 15 seconds, the STBY_COM! becomes 'low' and the receiver is switched to standby mode (see wireless mode).

9.12.4 Amplifier

This module can be used in two modes:

- Wireless mode
- Wired mode

9.12.4.1 Wireless mode

The amplified surround audio signal at the clickfits (diagram H2) can also be wired to the master box.
The input from the receiver is present at pin 2 of connector 1262 and fed via the emitter of TS7268 to the input of the amplifier. This signal can be connected to ground by TS7269 in case the STBY_COM! signal 'low' is. Pin 5 of 1262 is the mute pin.
When the MUTE is 'high', TS7270 conducts and pin 3 of comparator IC7262A becomes lower as the V_{REF} at pin 2 (4V6). As a result C2280 discharges via R3280. In wireless mode, the V_{REF} at pin 6 of IC7262B is 6V, and so it takes 15 seconds before pin 5 becomes lower as pin 6 of IC7262B. So in case the mute from the receiver is active for 15 seconds, by then the STBY_COM! will become 'low' and will switch the system to standby.

9.12.4.2 Wired mode

In case of wired use the switch in the cinch connector is open and so the supply voltage for the receiver at pin 3 of 1262 is not present any more. The audio signal - via pin 2 of plug 1260 - is fed to the AUDIO-IN! signal and to the low-level detector.
In wired use, the mute signal from the receiver-module should be disabled. If there is no voltage on pin 3 of 1262, pin 5 of 1262 will be forced high by R3305 and D6275 which means a mute state. This will force TS7270 in conduction as long as the wired mode is active. In this way D6276 is blocked and so the receiver-mute is disabled.
In the wired mode, a low-level detector is used, made by the circuitry around IC7260B and TS7260A. IC7260B and IC7206A are used as amplifier. The voltage divider R3320 and R3321 is used to limit the input signal to IC7260. C2269, C2295 and C2289 are used to block the DC-components. Via D6271 and D6272 only the positive pulses are fed though to pin 3 of comparator IC7262A. Only in case the audio level at the input of the low-level detector is lower as 3mV-RMS, pin 3 of comparator IC7262A becomes lower as the V_{REF} (4V6) at pin 2 and so the output at pin 1 IC7262A becomes 'low'.
As long as the input of the low-level detector is lower as 3mV-RMS, output pin 1 of IC7262A is 'low' and so C2280 is discharged via R3280. In case of a wired mode the threshold-level of comparator IC7262B is increased by a current through D6266 and R3277. As a result in wired mode the threshold level at pin 6 is decreased to 1V3. Therefor it takes 90 seconds before the discharged C2280 becomes lower than pin 6 of IC7262B. So only in case of 90 seconds no (or too low) sound, the STBY_COM! becomes 'low' and will switch the system to standby.

9.12.4.3 Amplifier

- IC7267 is the amplifier for both the master and the slave loudspeaker. It has an output power of 2x8W.
- To ensure a proper start up of the amplifier IC from standby to normal operation, pin 1 is used.
  Pin 1 filters the supply voltage at pin 12.
  * In normal operation STBY_COM! and so pin 6 of the IC is 'high' and so internally pin 12 is connected to pin 1.
  * In standby pin 6 is 'low' and so pin 12 is not connected any more to pin 1. During standby C2286 is precharged via the high STANDBY. This is done to realise a fast built up of the voltage at C2286 when the set is going from standby to normal operation in case of a bad charging of C2286 through IC7267.
- D6265 is used to charge C2282 to avoid plops at switching on.
- From normal operation to standby the following takes place in time:
  * Main supply of transformer L5513 is switched off inmediately, but C2314 is still charged.
  * Then C2290 is charged by the 'low' STBY_COM! signal and so - via the conducting TS7269 and TS7268 - the AUDIO-IN signal is muted.
  * Then C2284 is discharged by the 'low' STBY_COM! signal and so the standby pin 6 of amplifier IC7267 becomes 'low'. The amplifier is switched off after the AUDIO_IN is muted to avoid plops.
  * Then C2314 of the main supply is discharged and only the supply of L5312 is supplying energy to the stabiliser 7275.

DualScreen

9.13 Introduction

The wide picture version of the MD2.2 chassis can be provided with the DualScreen feature. In this there are two variants which can be distinguished:

- In the most basic version TXT or nexTView can be displayed next to the main picture. This is called 'text DualScreen'.
- In a higher specified sector it is possible, in addition to this, to display two video pictures simultaneously next to each other on the screen. This is called 'Video DualScreen'. When combined with text DualScreen this is designated as 'full DualScreen'.

Text DualScreen (video/TXT or video/nexTView)

The picture is divided into two, in a horizontal ratio of 60/40. These two parts are filled as follows:

- The video information is compressed horizontally and pushed left to the left-hand 60% of the picture by means of the PANIC on the Feature Box.
- The TXT or nexTView information is compressed horizontally and pushed right to the right-hand 40% of the picture by means of a circuit on the TXT+control module.

The total picture is further compressed vertically by means of the DDP.

Video DualScreen (video/video with sound of the second video picture on the headphones plug)

Two different video pictures are displayed next to each other in a horizontal ratio of 50/50, whereby the sound of the second video channel is fed to the headphone plug. This is achieved using the so-called 'video DualScreen' and 'YUV interface' modules and modified Dolby Audio Module:

- The 1fH YUV main signal is branched off immediately after TDA9143 on the SSP via the YUV interface panel and is fed to the Video DualScreen module.
- The 1fH YUV sub-signal from the second video picture is created on the Video DualScreen module by means of a 2nd tuner, an MF-demodulator and a TDA 9143.
- The YUV main and sub-signals are placed next to each other in the PIPO (Picture In Picture Out). The YUV output signal (YUV-DW) is still always on the base of 1fH and is fed back to the YUV interface. There is a YUV switch on the YUV interface:
  * If the Video DualScreen feature is not activated, the YUV main signal from TDA9143 on the SSP is immediately looped through to the Feature Box.
  * If the Video DualScreen feature is activated, the YUV-DW signal is fed to the Feature Box.

If the Video DualScreen feature is activated, the sound of the second video channel is fed to the headphones plug via a modified Dolby Audio Module.

9.14 Text DualScreen

9.14.1 Horizontal compression of the TXT/nexTView information (Fig. 9.14)

Principle

- SK1 and SK2 are components of the Blending circuit (see chapter Video Processing).
- The TXT information is compressed by the RGB info to be written into a memory and then read out on a double frequency.
- In order to be able to display the TXT information in the 40% screen, all level 2.5 features, including the side panel feature, are switched off by the software. The maximum number of characters which can be displayed per line is reduced from 56 to 40. Since nexTView also makes use of these possibilities it also has the result that the layout of this is modified in nexTView DualScreen mode.
- In order to set the analogue RGB signals at the correct digital level for the memory IC7462 (after all, this IC can only process digital information), an additional buffer has to be fitted between IC7462 and the TXT-IC, IC7400, namely IC7461. Because IC 7461 also inverts the signal, then after reading out from IC7462 an inverter IC7463 is used in order to 'straighten' the signal again.
- Because IC7461 discriminates the RGB (and FBL) level to high or low (no longer any interim steps) TXT level 2.5 colours (32 colours) is automatically returned to TXT level 1.5 colours (8 colours) if text DualScreen is active.
- With the DWE (Double Window Enable) switch line, originating from the operating mP, a selection is made between a complete TXT/nexTView picture or a DualScreen. If DWE is low, the text DualScreen is displayed.

Remark:
Due to the software suppression of level 2.5 features in DualScreen mode, then not only will the side panel feature be switched off but also the background colours, DRCS, etc.

Writing to and reading out of the memory

- The TMS4C1050B (IC7462) is a 4 bit organized memory. This memory is addressed via 2 independently operating reading and writing address counters. In addition to this the IC has a separate data write bus A and a separate data read bus B.
- The D0, D1, D2, D3 inputs are used to write the Blanking and RGB signals into the memory. The following signals are used to control the writing section:
  - ★ **W**rite enable (W) releases the write address counter and gives permission for data to be written into the memory.
  - ★ **ReSeT W**rite (RSTW) provides a reset for the write address counter.
  - ★ **S**erial **W**rite **C**loc**K** (SWCK) is a clock signal which determines the writing speed of the memory.
- The Q0, Q1, Q2, Q3 outputs are used to read out the Blanking and RGB signals from the memory.
  The following signals are used to drive the reading section:
  - ★ **R**ead enable (R) releases the read address counter and gives permission for data to be read out of the memory.
  - ★ **ReSeT R**ead (RSTR) provides a reset for the read address counter.
  - ★ **S**erial **R**ead **C**loc**K** (SRCK) is a clock signal which determines the reading speed of the memory.

In text DualScreen the frequency of the read clock is double that of the write clock.

Creating the clock signals in order to be able to read and write in the Field Memory

In order to provide the memory IC, IC7462, with the required clock pulses, the following circuits are made:

- The TXT-IC gives pin 39 a TCASIN with a frequency of 12 MHz with its harmonic. A band pass filter, with an adjustable coil L5465, only allows the 2nd harmonic to pass. This 24 MHz is used directly as a read clock (SRCK). In order to obtain a synchronous running writing clock (SWCK) which is exactly half the speed of the read clock, the signal is driven through a 2 divider IC7465/A.
- The TXT/IC delivers on pin 3 a line frequency pulse with a duty-cycle of exactly 50% (signal PL). This pulse is used as the clock input for the 2nd flip flop IC7465/B. The vertical flyback pulse (VFB) arrives on the D input. A reset read (RSTR) and a reset write (RSTW) are therefore generated at raster frequency. Since there is a time difference between the two trigger points (rising slope) of these reset signals, the 12 MHz clock is held up to the START moment. In this way the writing and reading are exactly synchronized.
- At the START moment the RSTR is high. As a result of this the 12 MHz write clock is released and the writing into the memory begins. This is exactly at the rising PL slope. The writing is now no longer interrupted until a further frame flyback. A full raster is therefore written into the memory.
- The reading of the memory is stopped just at the moment of START (Read enable is low). Only in the second half of the PL pulse (this is a half line time later) does the Read Enable become high. As a result of this the read address counter is released and the reading out of the memory starts. Since the read address counter is running at 24 MHz clock this reading out runs twice as fast as the writing. Another half a line time later the Read Enable again becomes low and reading out stops again.
  This cycle repeats itself for each line.
  - ★ During the first half of the line the PL is high, the read enable (R) is therefore low; nothing is therefore read out.
  - ★ During the second half of the line the PL is low and the memory is read out at double speed (24 MHz clock)

9.14.2 Horizontal compression of the video information

In addition to the compression of the TXT/nexTView section, the video section of the picture should also be compressed. For text DualScreen this horizontal compression is achieved by the PANIC IC in the FBX. Via a software command the picture is compressed in the PANIC and pushed horizontally to the left.

9.14.3 Horizontal centring of text DualScreen

In order to arrange the video and TXT/nexTView information neatly at the correct distance beside each other, initially the TXT/nexTView half on the right is set against the side of the picture by the DDP. After this, by means of the software centring of the FBX, the video half is set to the correct horizontal distance with regard to the TXT/nexTView information.

9.14.4 Vertical compression of the text DualScreen picture

The total picture for text DualScreen is compressed vertically with the aid of the DDP (vertical deflection is adjusted) in order to again obtain the correct height/width ratio of the video picture. As a result of this black bars are created on the top and bottom of the picture.

9.15 Video DualScreen

9.15.1 Introduction

The video DualScreen picture consists of 2 sections of the same size:

- the left-hand section is the main picture originating from the main tuner or from RGB, CVBS or SVHS signals from external sources.
- the right-hand section is the sub-image originating from the 2nd tuner or from CVBS or SVHS signals (no RGB signals) from external sources. The video decoding for the sub-image takes place on the Video DualScreen module and makes no use of the COMB filter. The result is that the picture quality of the sub-image is generally less than that of the main picture.

9.15.2 Block diagram

The following blocks can be distinguished on the Video DualScreen:

- PLL tuner E9F1 is a UV1216D which is driven via I^2C.
- A TDA9815 is used for MF demodulation.
  The PCF8574AT controller IC9N is used in order to set the switching signals from the MF demodulator into the correct mode.
- Via a source selector IC9L a selection is made between TUN_CVBS (from the Video DualScreen tuner) or CVBS PIP (from the TEA6415 source selector on the SSP). At the same time this IC9L can be used to select between CVBS-PIP or YC-PIP.
- The Y/CVBS-PIP or CVBS TUNER signal and the C-PIP signal are fed to the TDA9143 IC9J on the Video DualScreen module. Together with the delay line IC9K the CVBS or SVHS signal is converted here to the SUB-YUV signals together with the sync signals SPHsync and SPVsync. The RGB-TXT inputs of this TDA9143 are not used here.
- The sub-YUV signals (SY, SU, SV) together with their sync signals SPVsync and SPHsync and the Main-YUV signals (MU, MY, MV) with their sync signals HA = SC_1fH = DPVsync are placed next to each other in the PIPO (Picture In Picture Out) IC9A SAB9077. The RAM IC9E is used as the memory.
- The output of the SAB9077 DW-YUV signals (DY, DU, DV) are fed directly to the output of the Video DualScreen panel to the YUV interface (in the MD2.2 the function of the switching IC IC9M is on the YUV interface, therefore IC9M and the switching signals DFB1 and DFB2 are not used). Via the switching signal FBLK the YUV interface can be set to the bypass mode (FBLK 'low') or to the Video DualScreen mode (FBLK 'high').
- If the Video DualScreen feature is not active, part of the +5V supply voltages (+5VSW) is switched off via Q9N1 and switching signal VDS STANDBY (VDS STANDBY becomes 'low' (standby mode) 60 seconds after the VDS feature is switched off. As a result of this the load of the +5V supply voltage reduces if the Video DualScreen feature is not used. Because the PIPO is also switched off, then via IC9P and VDS TSNADBY = 'low', the HA and VA sync signals are not looped through to the HA' and VA' sync signals which go to the PIPO. This prevents the non-active PIPO loading the HA and VA signals.
- Because the TXT/nexTView DualScreen are created by a totally different signal path in the MD2.2, connector J9A5, J9A6, the buffers around Q9P1, Q9R1 and Q9S1 and the section of pin 12, 13, 14 of IC9L are not used.

9.15.3 Tuner and MF section

The tuner is an I^2C controlled PLL tuner with built-in splitter. The antenna input goes to the Video DualScreen module and is split there into the main and Video DualScreen tuner. The D_TUN pin 8 is the supply for the splitter section. The ADDRESS pin 15 is used to give this tuner a different address on the I^2C bus of the main tuner.

The MF section can handle all of the systems throughout the world and is constructed around the MF demodulator IC9R, the TDA9815 (also used in GR2.4). This is, with regard to pinning, the same as the TDA9811 of the MD2 MF module, however, in the TDA9815 an FM demodulator is built in. In order to select the correct demodulation system and the correct filtering, the following switching signals are used. These switching signals originate from the PCF8574AT IC9N.

System	BG/LL'IMDK	L'	I	POS/NEG	M
BG	1	0	0	1	0
L	0	0	0	0	0
L'	0	1	0	0	0
I	0	1	1	1	0
M	0	0	0	1	1
DK	0	0	0	1	0

The video path

- *BG via SAW filter FL90*
  BG/LL'IDKM is 'high', D9G0 conducts, D9G1 reverses. As a result of this IF2 becomes short-circuited and IF1 is fed to the Video IF inputs pin 1 and 2 of the TDA9815 via the BG SAW filter FL90.
- *LL'IDK via SAW filter FL91*
  BG/LL'IDKM is 'low', D9G0 reverses, D9G1 conducts. As a result of this IF1 becomes short-circuited. Because M-TRAP is 'low', D6G2 reverses and D9G3 conducts as a result of which the IF2 is fed to the LL'IDK SAW filter FL91.
  At the same time D9G5 conducts and D9G4 reverses because M-TRAP is 'low'. As a result of this pin 4 and 5 of FL92 (M SAW filter) become short-circuited and pins 5 and 4 of FL91 (LL'IDK SAW filter) are not short-circuited. Therefore, pins 5 and 4 of FL91 are looped through to pins 4 and 5 of TDA9815 respectively.
  The circuit around L9F2 filters out the sound at 40.4 MHz from the adjacent channel.
- *M via SAW filter FL92*
  BG/LL'IDKM is 'low', D9G0 reverses, D9G1 conducts. As a result of this IF1 becomes short-circuited. Because M-TRAP is 'high', D6G2 conducts and D9G3 reverses as a result of which the IF2 is fed to the M SAW filter FL92.
  At the same time D9G5 reverses and D9G4 conducts because M-TRAP is 'high'. As a result of this pins 4 and 5 of FL91 (LL'IDK SAW filter) are short-circuited and pins 5 and 4 of FL92 (M SAW filter) are not short-circuited. Therefore, pin 4 and 5 of FL92 are looped through to pins 4 and 5 respectively of the TDA9815.
- Pin 30 selects the MF inputs: 'high' for the BG VIF inputs pin 1-2 and 'low' for the LL'IDKM VIF inputs pin 4-5.

- In order to filter sound from the Video IF (VIF), the series connected band reversing filters X9T4, X9T5 and X9T6 are used. X9T4 is only connected in series in the M mode (M-TRAP 'high' therefore Q9F5 reverses and Q9F6 conducts). Pin 21 is the output, pin 22 the input. Finally, the buffered TUN-CVBS signal is present on pin 10.
- AFC oscillator between pins 23 and 24 which is adjusted to 77.8 MHz (2 x 38.9 MHz). The adjustment takes place via pin 23 of the AFC detector. The AFC loop of the Video DualScreen demodulator is not used. The AFC loop of the main demodulator on the IF module of the set itself is used to correct any drift of the transmitter for both the main tuner and for the Video DualScreen.
- Pin 9 is 'high' for BGIDKM (negative modulation) and 'low' for LL' (positive modulation).
- Pin 11 is 'low' in the L' mode (L' 'high') or in the M mode (M-TRAP 'high') via Q9F1. A low pin 11 is interpreted in the positive modulation mode (pin 9 'low') in order to de-tune the 38.9 MHz to 32.4 MHz. In the negative modulation mode (pin 9 'high') a low pin 11 is interpreted in order to select sound input pin 18 (M audio input) instead of the sound input pin 17 (BGLL'IDK audio input).
- Pin 7 is switchable for the PLL loop filter. For BGIDKM, R9H9 is short-circuited via Q9F2 as a result of which the time constant is changed.
- Pin 6 is used in order to adjust the AGC takeover point via R9H5.

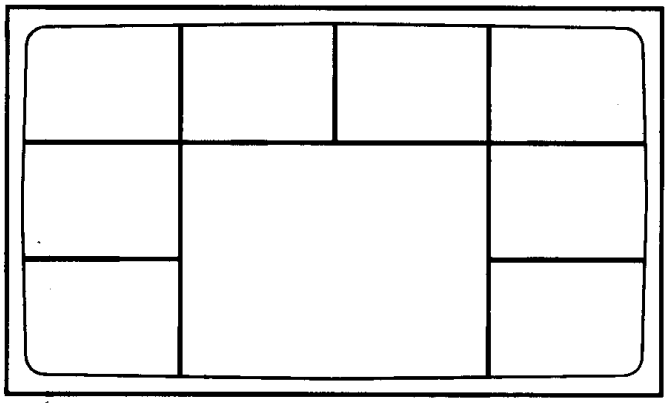
The sound path

The TDA9815 delivers an FM mono or AM mono. Via L9F8 the sound path is disconnected from the picture path.

- *BG via SAW filter FL93*
  L' is 'low', D9G8 conducts, D9G9 reverses, pin 6 of the L9F8 is short-circuited via C9T5. Therefore, the MF signal from the tuner is fed via pin 4 of L9F8 to pin 1 of FL93 (BG SAW filter) and pin 2 of FL94 (LIDK SAW filter). Because BG/LL'IMDK is 'high', D9G6 conducts and D9G7 reverses. As a result of this pins 4 and 5 of FL94 (LIDK SAW filter) are short-circuited and pins 5 and 4 of FL93 (BG SAW filter) are not short-circuited. Pins 5 and 4 of FL93 (BG SAW filter) are looped through to pins 31 and 32 of TDA9815 respectively.
- *LIDK via pin 2 SAW filter FL94*
  L' is 'low', D9G8 conducts, D9G9 reverses, pin 6 of the L9F8 is short-circuited via C9T5. Therefore, the MF signal from the tuner is fed via pin 4 of L9F8 to pin 1 of FL93 (BG SAW filter) and pin 2 of FL94 (LIDK SAW filter). Because BG/LL'IMDK is 'low', D9G6 reverses and D9G7 conducts. As a result of this pins 5 and 4 of FL93 (BG SAW filter) are short-circuited and pins 5 and 4 of FL94 (LIDK SAW filter) are not short-circuited. Pins 5 and 4 of FL94 (LIDK SAW filter) are looped through to pins 32 and 31 of TDA9815 respectively.
- *L' via pin 1 SAW filter FL94*
  L' is 'high', D9G8 reverses, D9G9 conducts, pin 4 of the L9FB is short-circuited via C9T5. Therefore, the MF signal from the tuner is enabled via pin 6 of L9F8 to pin 1 input of FL94 (L' SAW filter). Because BG/LL'IMDK is 'low', pins 4 and 5 of FL94 are looped through to pins 31 and 32 of TDA9815 respectively.
- *M sound inter-carrier*
  In M mode the sound inter-carrier is processed, therefore the sound is extracted from the VIF information. Because the sound path is not used it is disabled by Q9F7.
- In order to filter the sound signal (SIF) from the picture the band reverse filters X9T0, X9T1, X9T2 and X9T3 are used. Pin 20 is the output, pin 18 the input for M sound and pin 17 the input for BGLL'IDK sound. Filter X9T1 (6.0 MHz) is switched off in the BG mode in order to prevent any NICAM BG carrier (5.85 MHz) from passing and filter X9T2 (6.5 MHz) is switched off in the I mode in order to prevent any NICAM I carrier (6.552 MHz) from passing.
- Pin 12 is the DW-MONO output. Via Q921 the de-emphasis for BGIDKM can be modified and additionally modified for M via Q922.

9.15.4 MultiScreen with the PIPO

In a set with the Video DualScreen module, Multi PIP is no longer created but MultiScreen is created with the aid of the PIPO SAB9077. In the MD2.2 the following configuration is selected:



76532013_010.AI
060397

For this the large picture is the main picture from the main tuner. The 8 small pictures are created by the Video DualScreen tuner. At the same time a scan or photofinish can be created with the 8 small pictures, for which the picture at the bottom right is the live picture.

Blockschaltbild nicht Top-Dolby-Version /

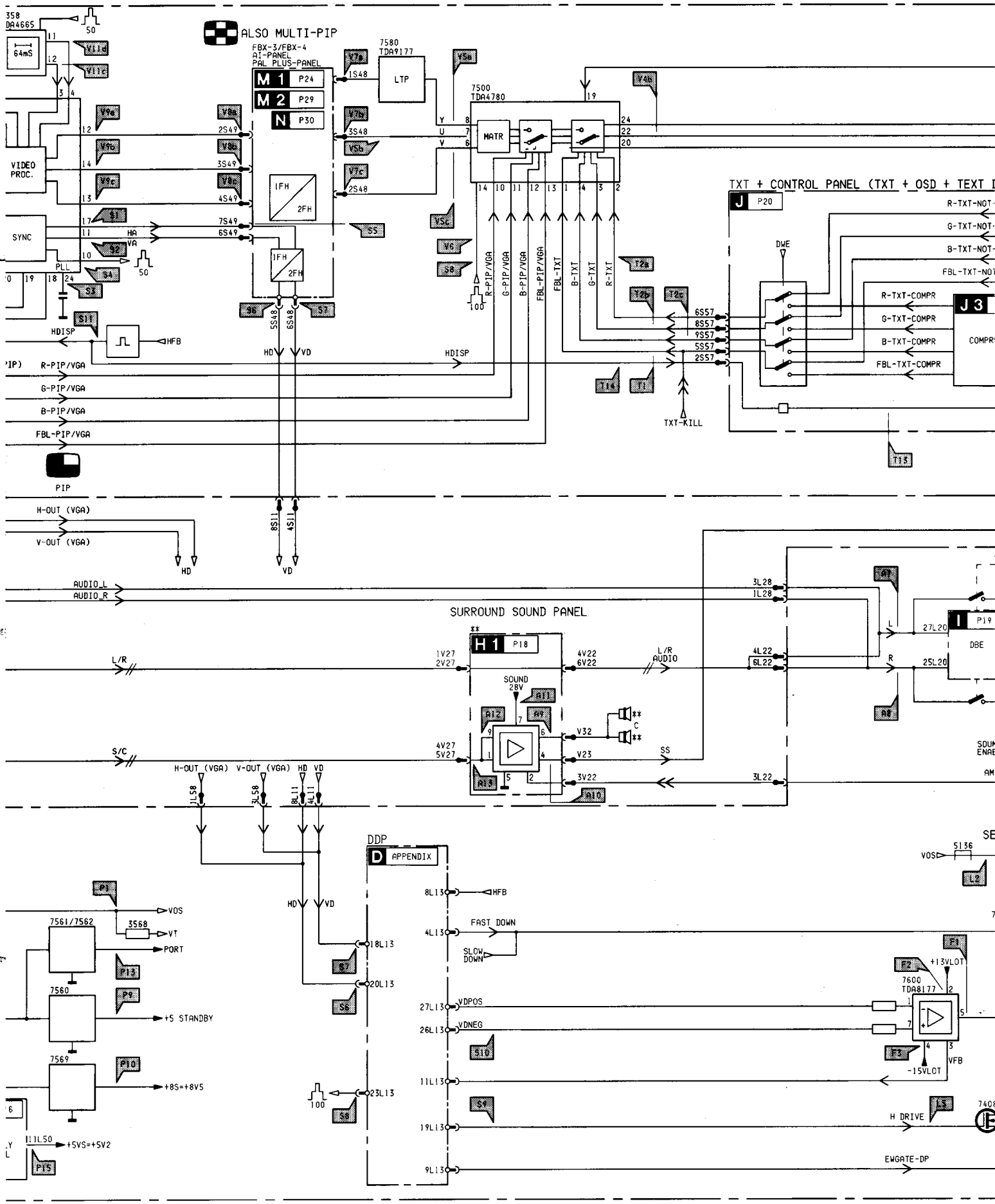
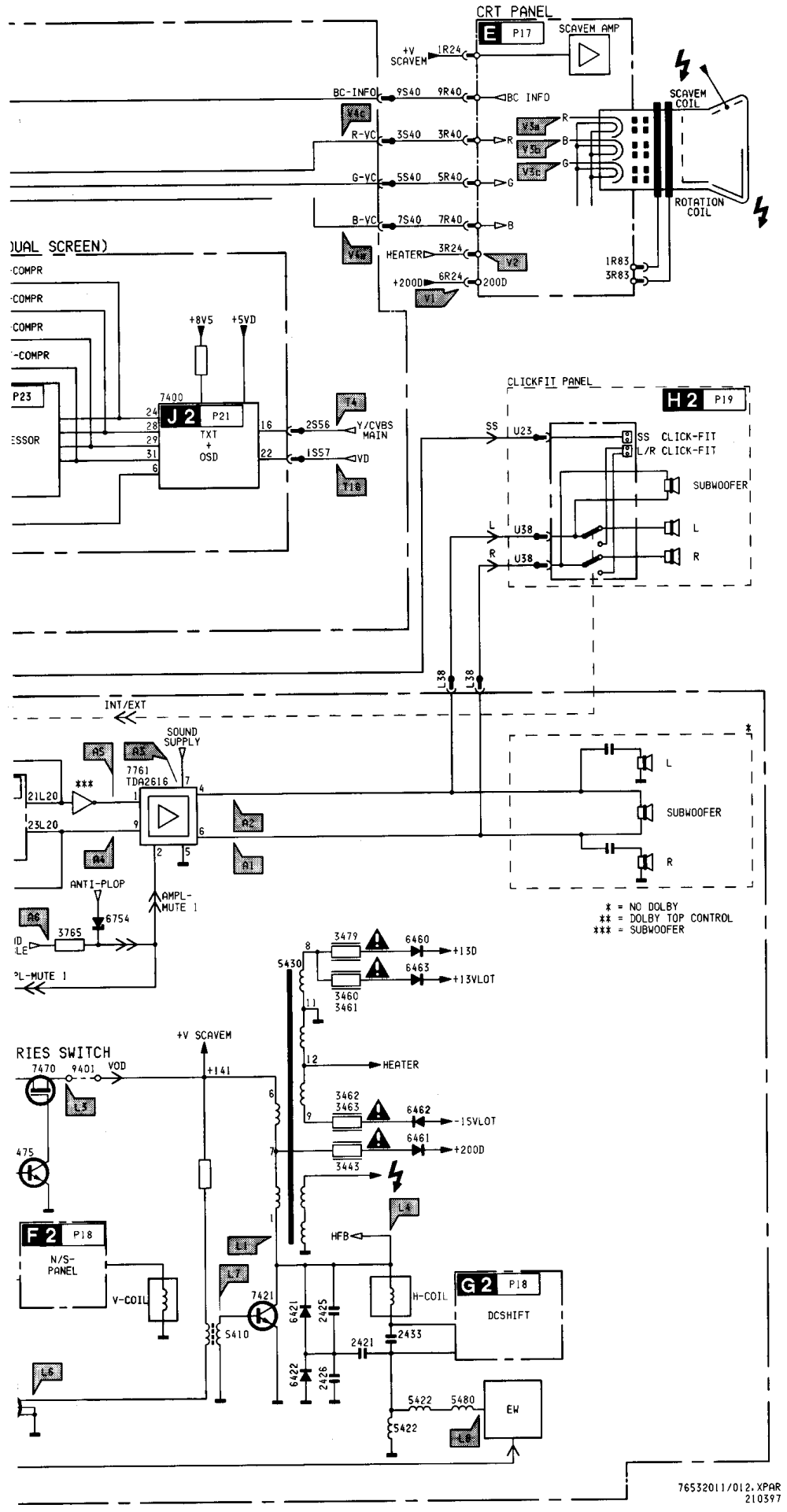
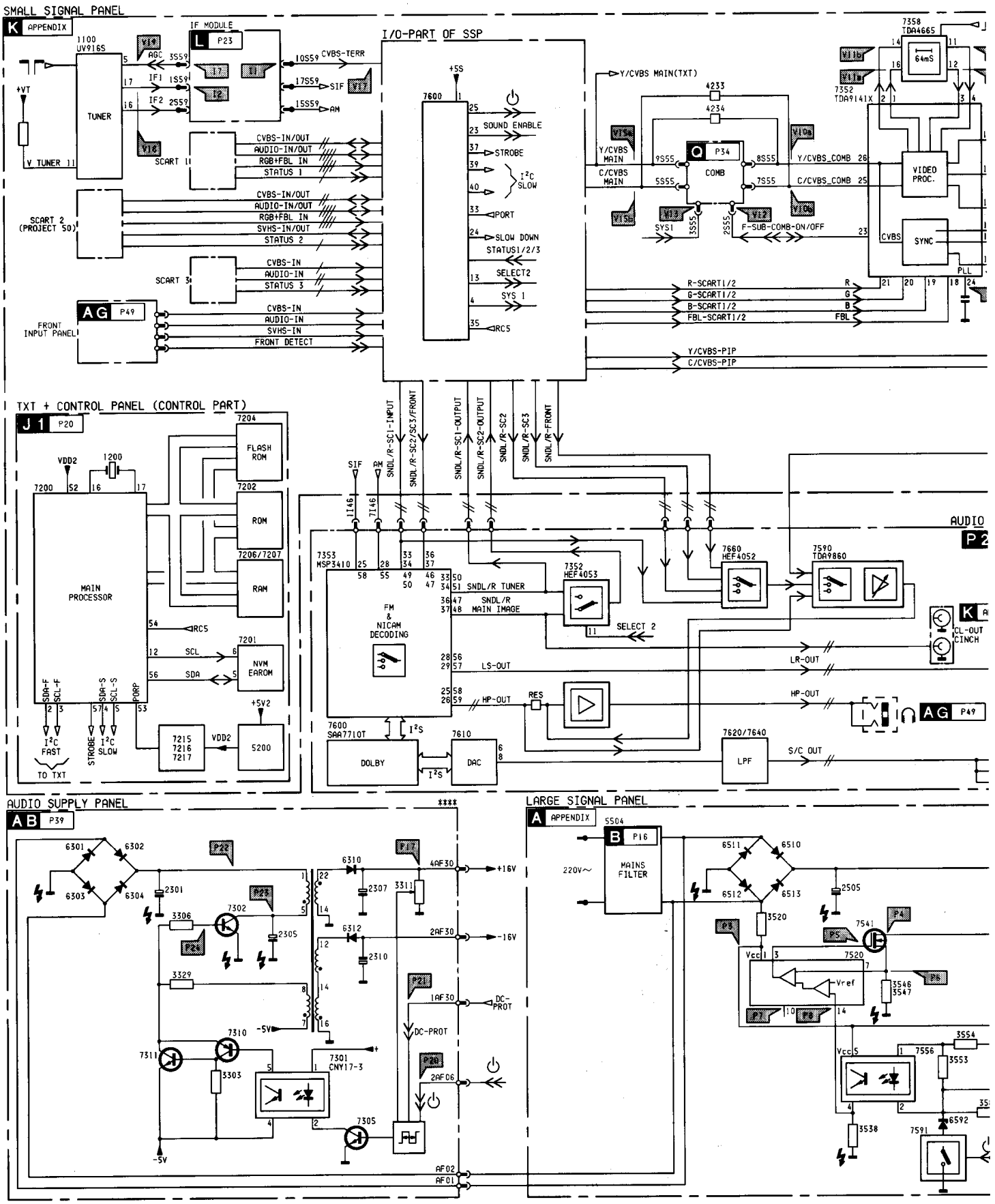


Diagramme synoptique version non Top-Dolby



Block diagram Top-Dolby version (front control styling) /



Blockschaltbild der Top-Dolby-Version /

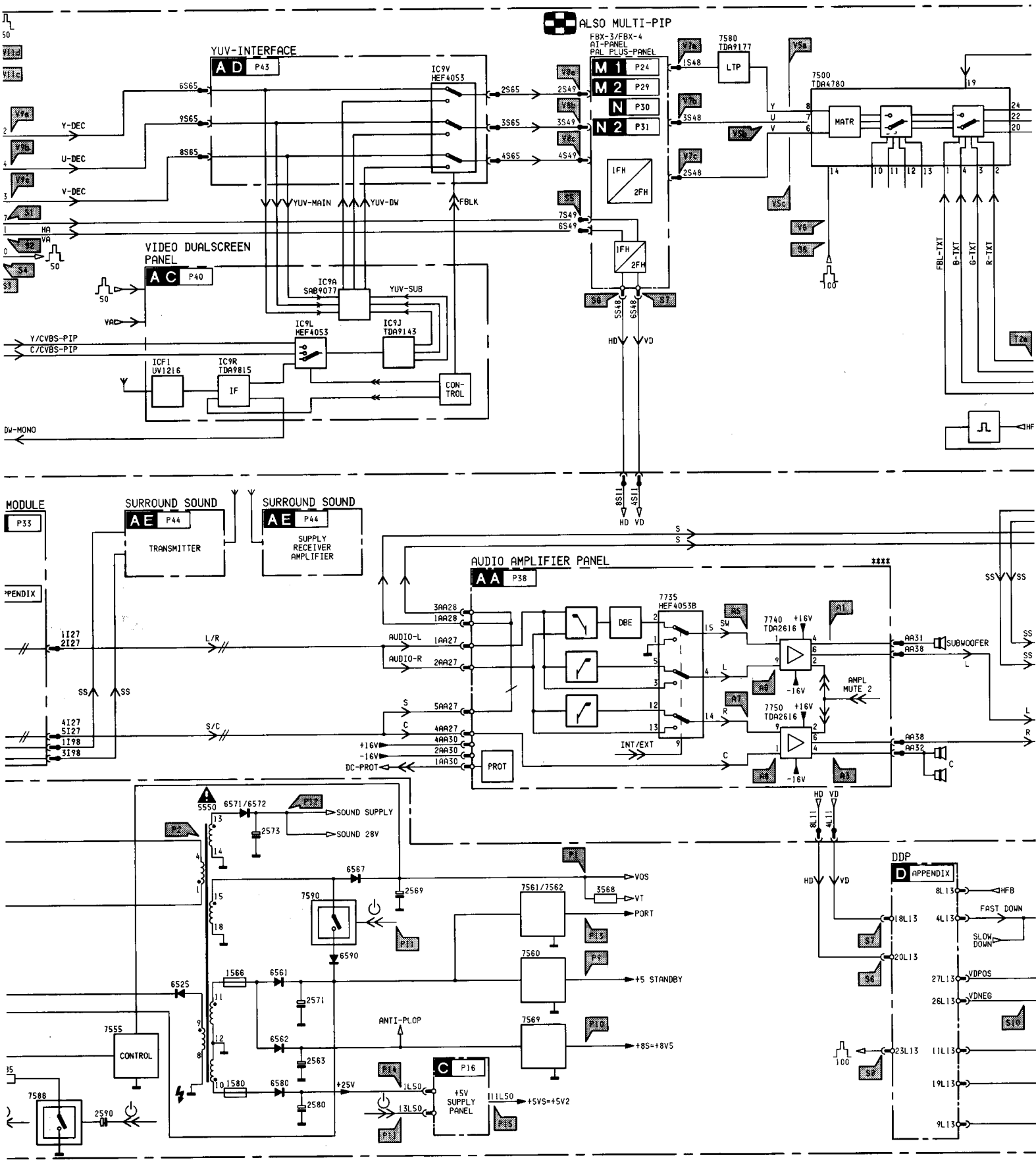
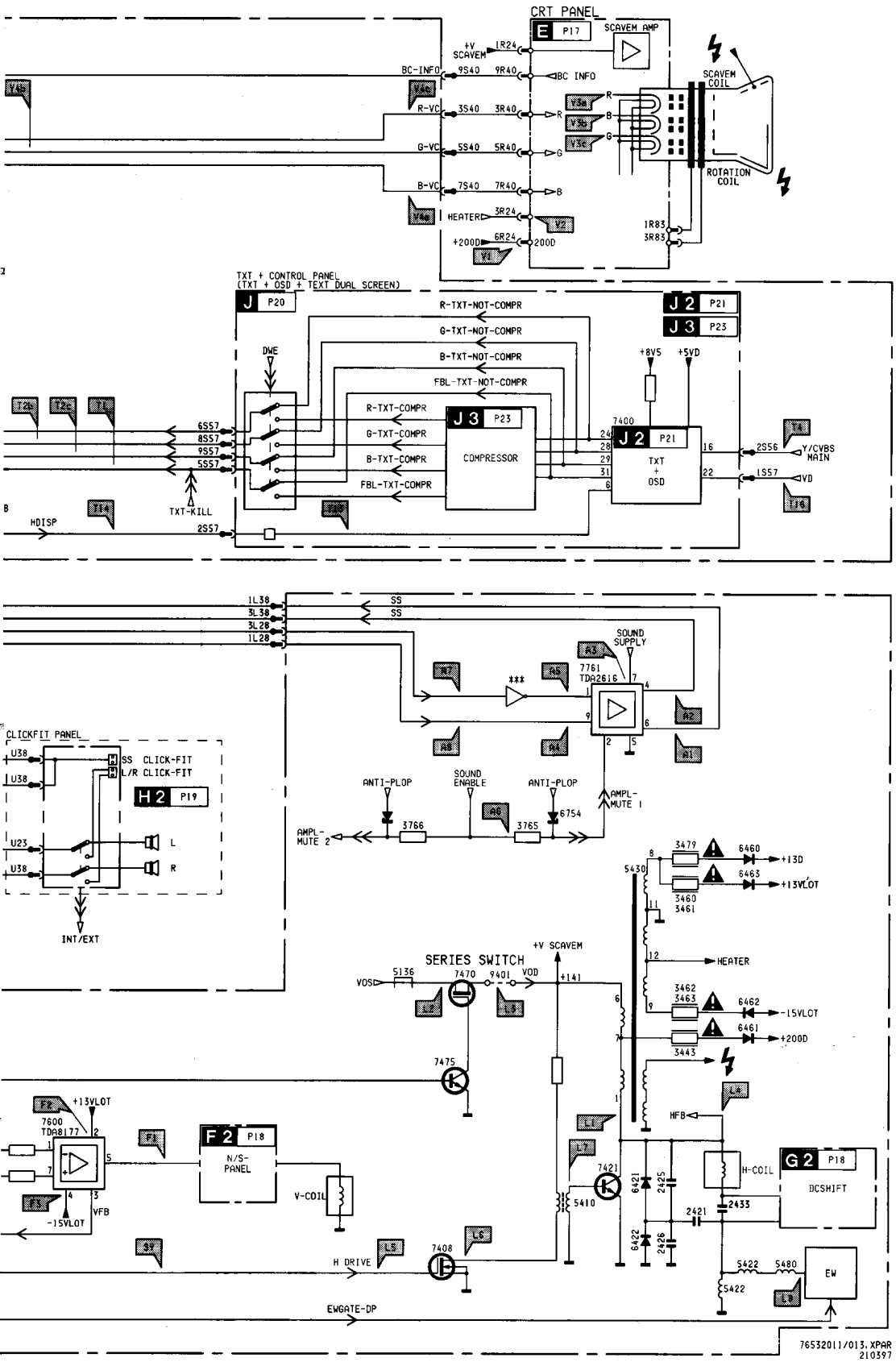


Diagramme synoptique de la version Top-Dolby



002	K6	7480	D4	3523	I9	5567	F6	9427	I5	9618	D3	2596	D7		
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004	B8	7520	I9	3526	I9	5573	D10	9429	H4	9620	A2	2609	C5		
005	F7	7541	J7	3527	I9	5617	E2	9431	H2	9621	C2	2612	D1		
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2400	G4	7560	E9	3530	J10	6409	N3	9433	H3	9624	A4	2614	D2		
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2433	H3	L10	E10	3541	J7	6460	J1	9447	E3	9759	A9	2753	B6		
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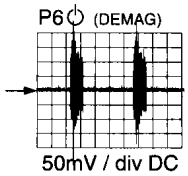
6572	F7	3517	L9	5542	J7	9422	H6	9612	D1	2590	F10				
6573	E6	3518	I9	5543	F7	9423	H5	9613	C1	2591	F10				
7421	L5	3519	K10	5544	I7	9424	H4	9615	A3	2592	D6				
7470	F5	3521	J9	5545	I6	9425	H5	9616	B3	2593	F6				
7475	E4	3522	K8	5561	D8	9426	L5	9617	A3	2594	F7				

POWER SUPPLY

P1 ⏀ (VOS)
140V DC

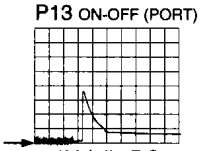
P1 ⏻ (VOS)
0V DC

P6 ⏻ (DEMAG)



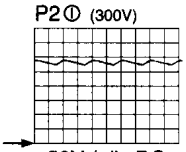
50mV / div DC
0.1s / div

P13 ON-OFF (PORT)



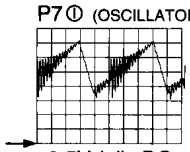
1V / div DC
1s / div

P2 ⏀ (300V)



50V / div DC
5ms / div

P7 ⏀ (OSCILLATOR)



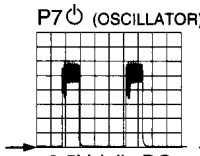
0.5V / div DC
5µs / div

P14 ⏀ (+25V)
27V5 DC

P2 ⏻
300V DC

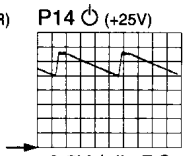
P3 ⏀ (Vcc IC7520)
14V DC

P7 ⏻ (OSCILLATOR)



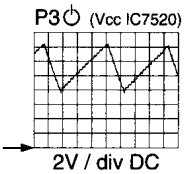
0.5V / div DC
0.1s / div

P14 ⏻ (+25V)



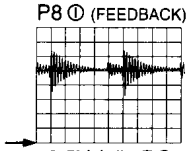
0.5V / div DC
20ms / div

P3 ⏻ (Vcc IC7520)



2V / div DC
20ms / div

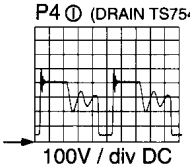
P8 ⏀ (FEEDBACK)



0.5V / div DC
5µs / div

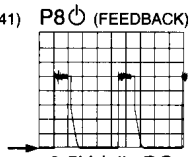
P15 ⏀ (+5S)
25V DC

P4 ⏀ (DRAIN TS7541)



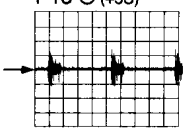
100V / div DC
5µs / div

P8 ⏻ (FEEDBACK)



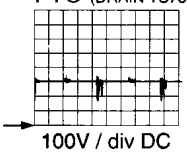
0.5V / div DC
20ms / div

P15 ⏻ (+5S)



20mV / div DC
20ms / div

P4 ⏻ (DRAIN TS7541)



100V / div DC
0.1s / div

P9 ⏀ (+5V STANDBY)
4V9 DC

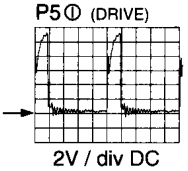
P9 ⏻ (+5V STANDBY)
4V9 DC

P10 ⏀ (+8S)
8V6 DC

P10 ⏻ (+8S)
0V DC

HORIZONTAL (LINE)

P5 ⏀ (DRIVE)

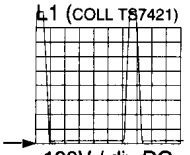


2V / div DC
5µs / div

P11 ⏀ (STANDBY)
3V9 DC

P11 ⏻ (STANDBY)
0V1 DC

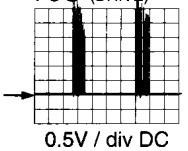
L1 (COLL TS7421)



100V / div DC
5µs / div

P12 ⏀ (SOUND-SUP.)
29V5 DC

P5 ⏻ (DRIVE)



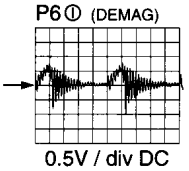
0.5V / div DC
0.1s / div

P12 ⏻ (SOUND-SUP.)
3V DC

L2
(TS7470 series switch)
140V9 DC

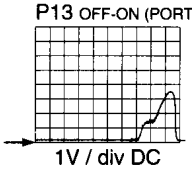
L3
(TS7470 series switch)
140V4 DC

P6 ⏀ (DEMAG)



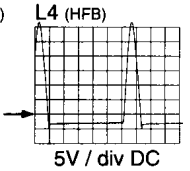
0.5V / div DC
5µs / div

P13 OFF-ON (PORT)



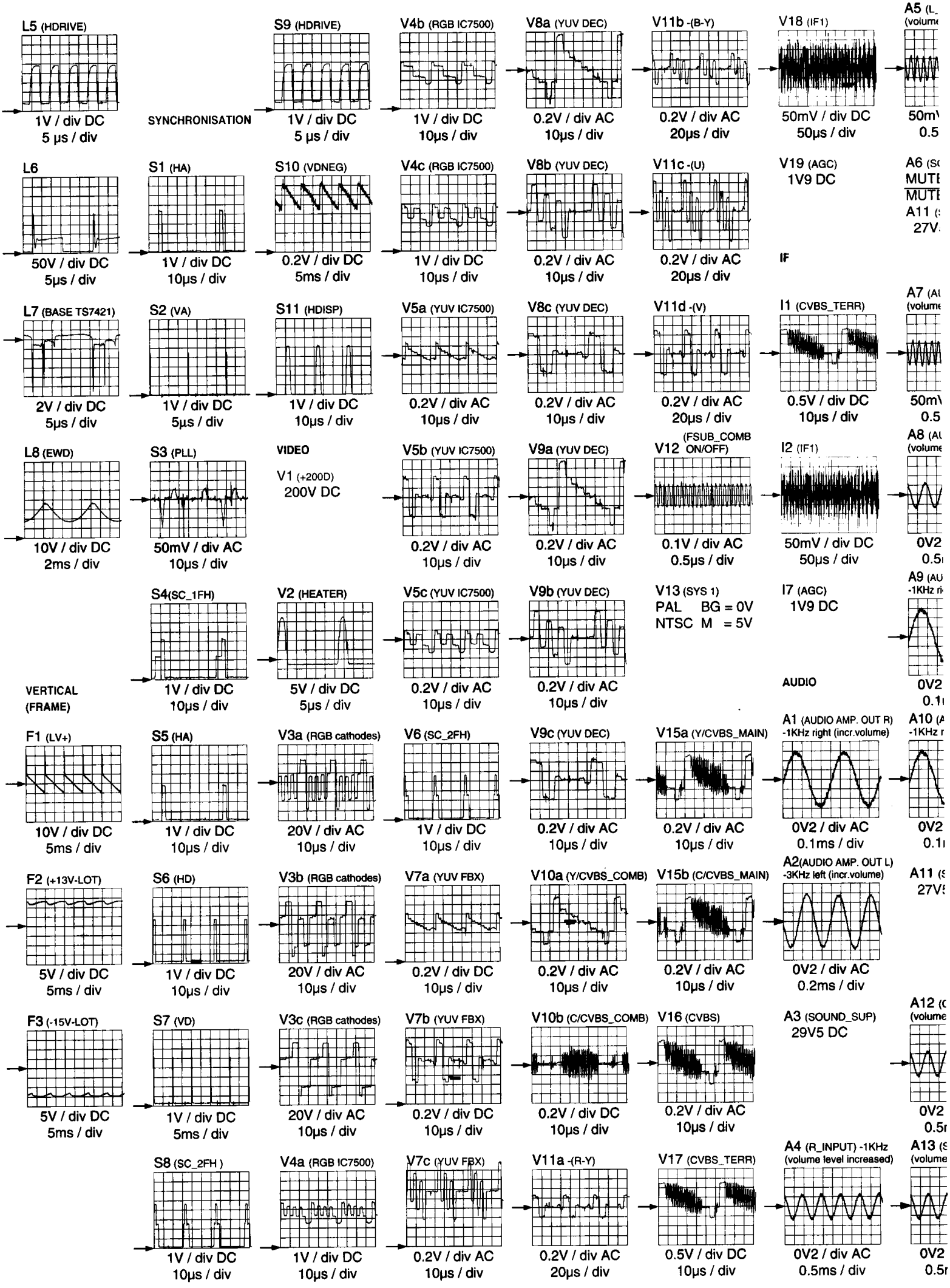
1V / div DC
20ms / div

L4 (HFB)

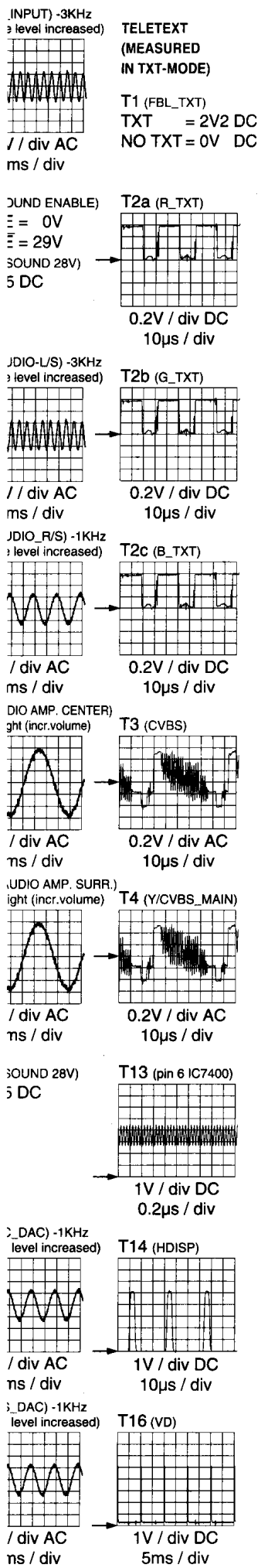


5V / div DC
5µs / div

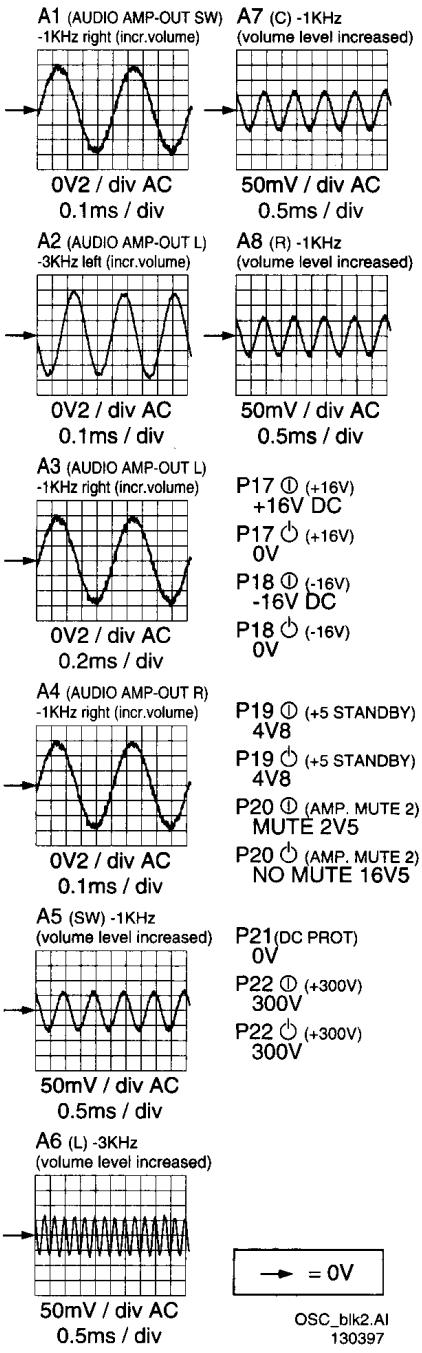
Overview oscillograms / Übersicht der Oszillogramme /



Vue d'ensemble des oscillogrammes



OSC_BLK1.AI
250297



OSC_blk2.AI
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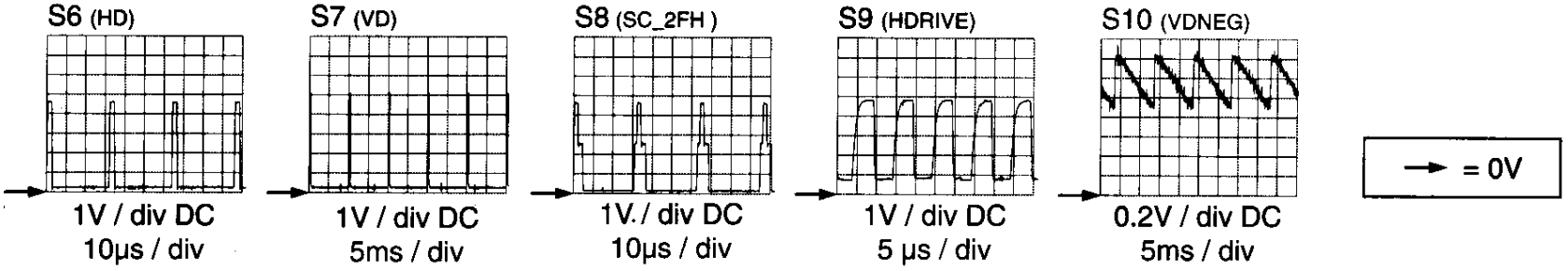
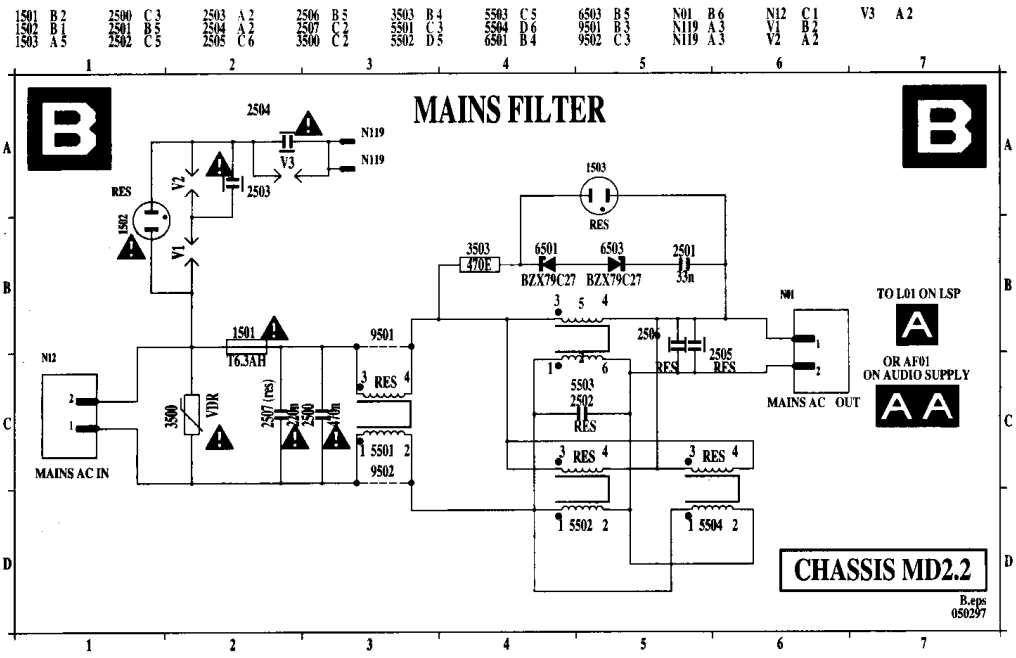
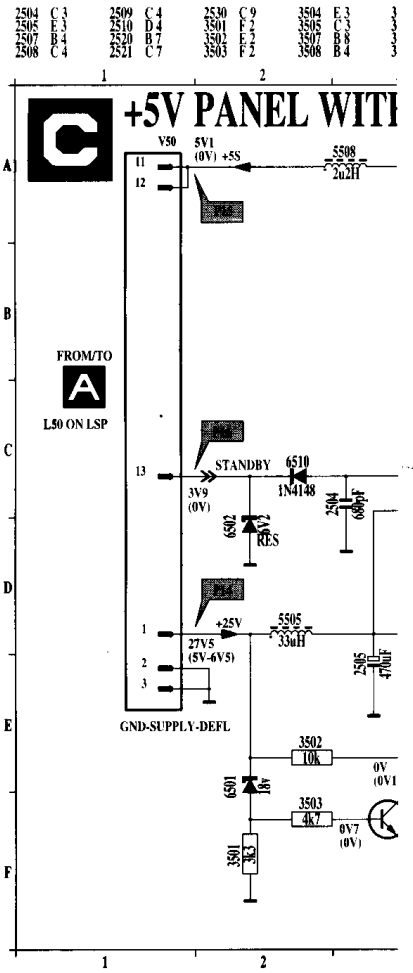


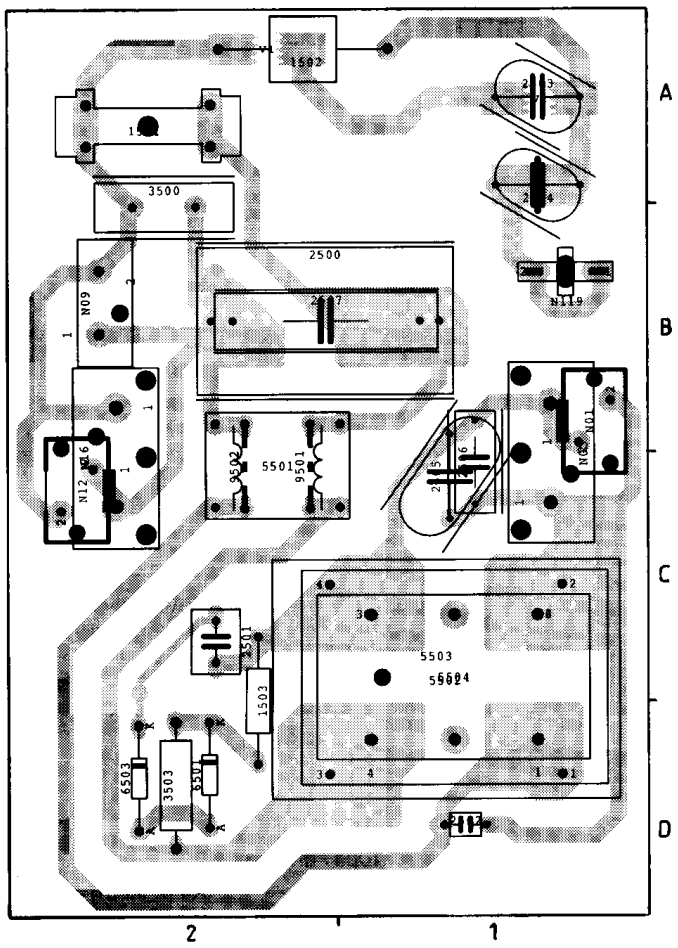
OSC_B.AI
180396

See appendix for circuit diagram LSP & SSP & DDP

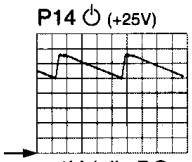
Mains filter panel / Netzfilterplatine / Platine filtre d'alimentation



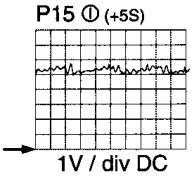




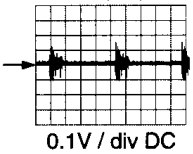
P14 ⏻ (+25V)
27V5 DC



P14 ⏻ (+25V)
1V / div DC
0.1s / div

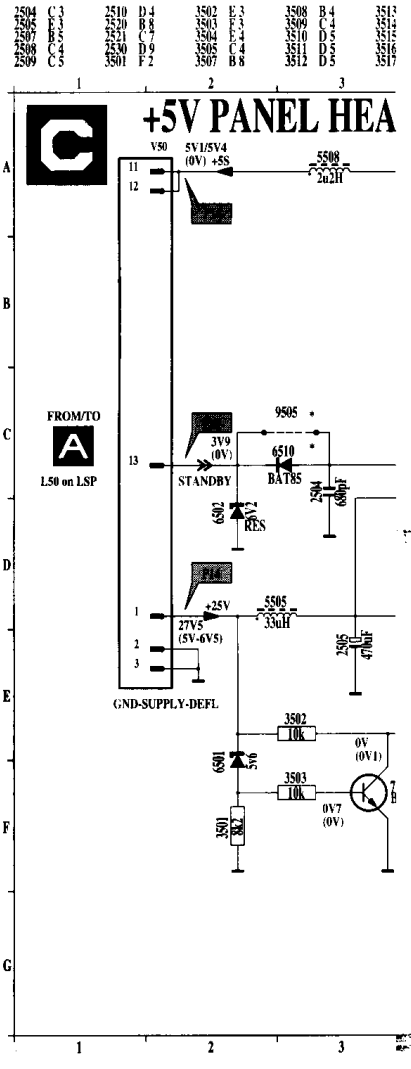


P15 ⏻ (+5S)
1V / div DC
10µs / div



P15 ⏻ (+5S)
0.1V / div DC
0.1s / div

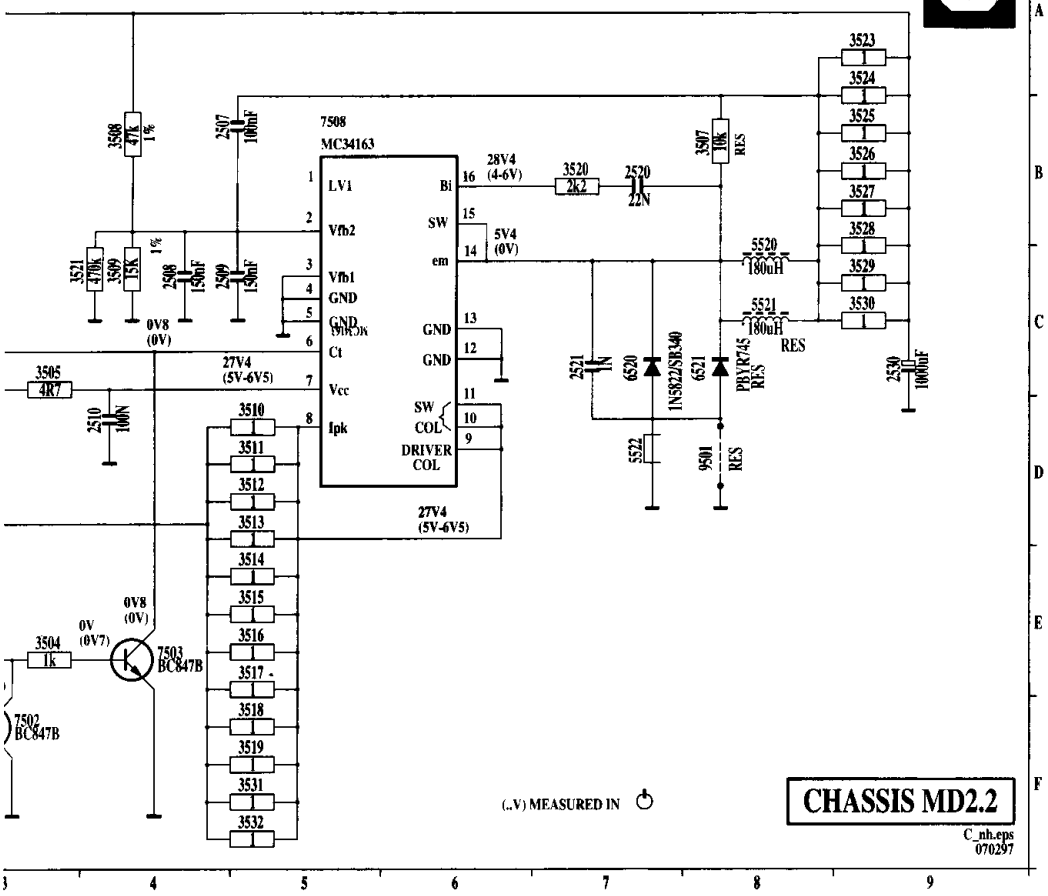
→ = 0V



OSC_C.AI
110397

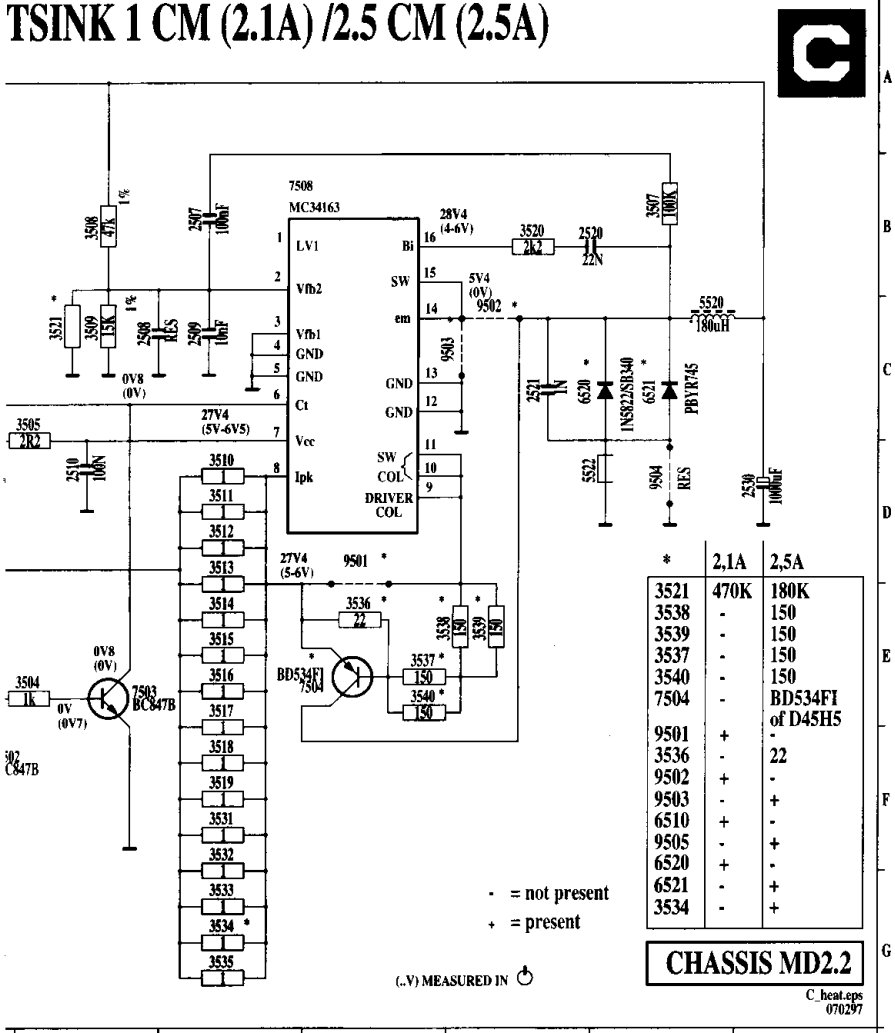
3509	C 4	3513	D 5	3517	E 5	3521	C 4	3526	B 9	3530	C 9	5508	A 3	6501	E 2	6521	C 8	9501	D 8
3510	D 5	3514	E 5	3518	F 5	3523	A 9	3527	B 9	3531	F 5	5520	C 8	6502	D 2	7502	F 3	V50	A 1
3511	D 5	3515	E 5	3519	F 5	3524	A 9	3528	B 9	3532	F 5	5521	C 8	6510	C 2	7503	E 4		
3512	D 5	3516	E 5	3520	B 7	3525	B 9	3529	C 9	5505	D 2	5522	D 7	6520	C 7	7508	B 5		

HOUT HEATSINK



D 5	3518	F 5	3532	F 5	3537	E 6	5508	A 3	6510	C 3	7504	E 6	9504	D 8
E 5	3519	F 5	3533	G 5	3538	E 7	5520	C 8	6520	C 7	7508	B 5	9505	C 3
E 5	3520	B 7	3534	G 5	3539	E 7	5522	D 8	6521	C 8	9501	D 6	V50	A 2
E 5	3521	C 4	3535	G 5	3540	E 6	6501	E 2	7502	F 3	9502	C 7		
E 5	3531	F 5	3536	E 6	5505	D 3	6502	D 2	7503	E 4	9503	C 7		

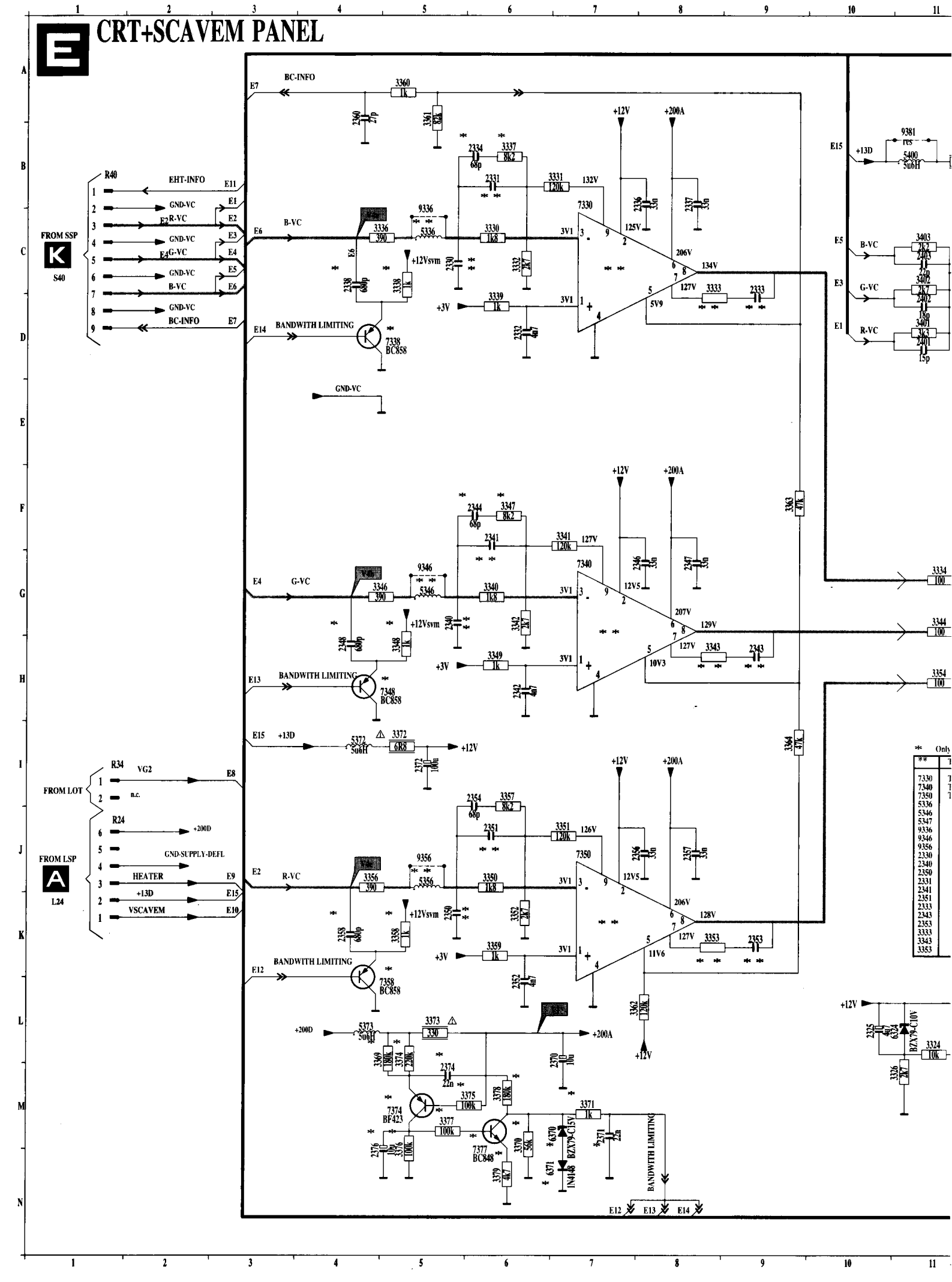
TSINK 1 CM (2.1A) /2.5 CM (2.5A)



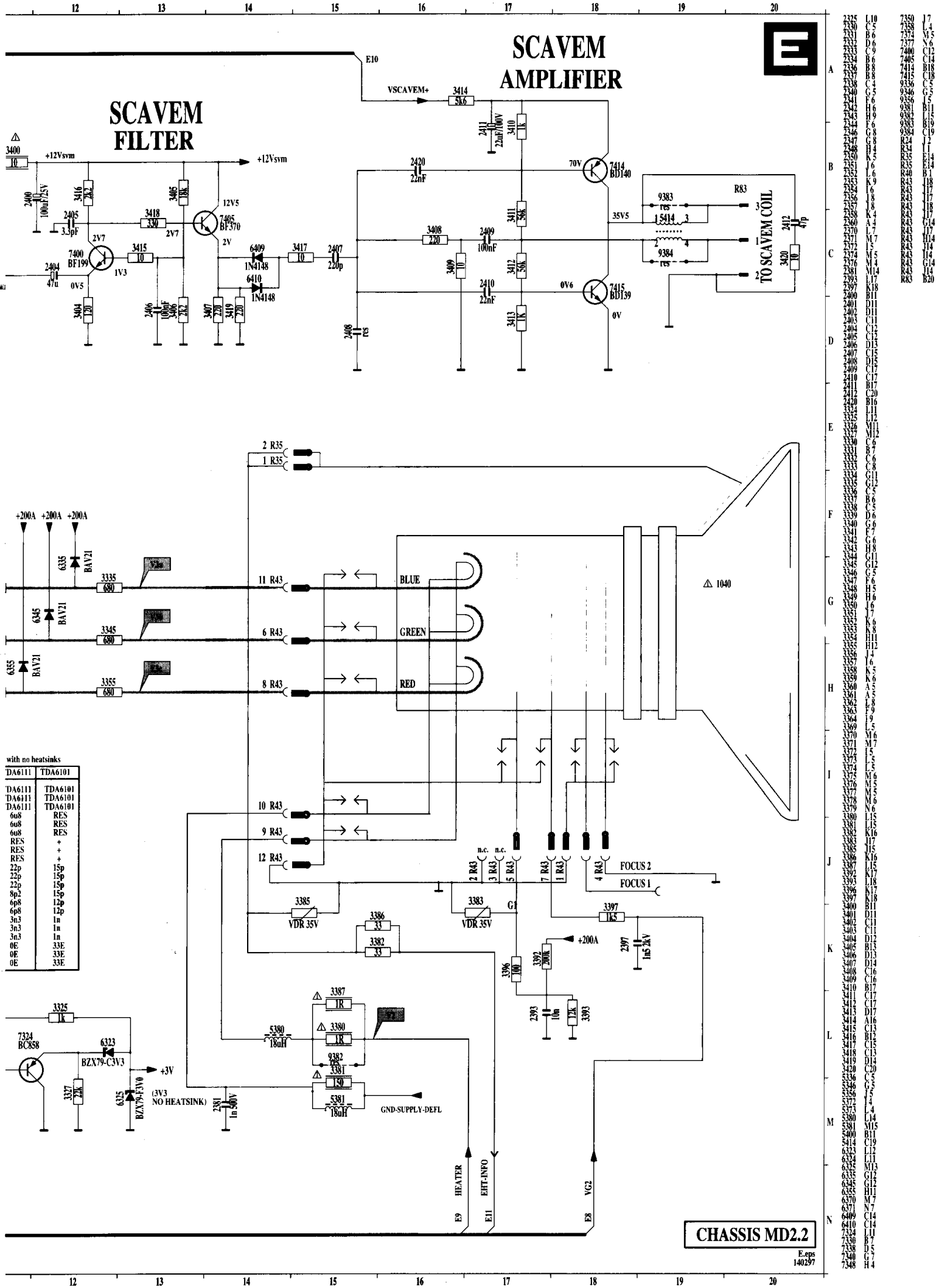
*	2,1A	2,5A
3521	470K	180K
3538	-	150
3539	-	150
3537	-	150
3540	-	150
7504	-	BD534FI of D45H5
9501	+	-
3536	-	22
9502	+	-
9503	-	+
6510	+	-
9505	-	+
6520	+	-
6521	-	+
3534	-	+

CHASSIS MD2.2

0050	A	1
2504	B	1
2505	B	2
2507	A	1
2508	A	1
2509	A	1
2510	B	1

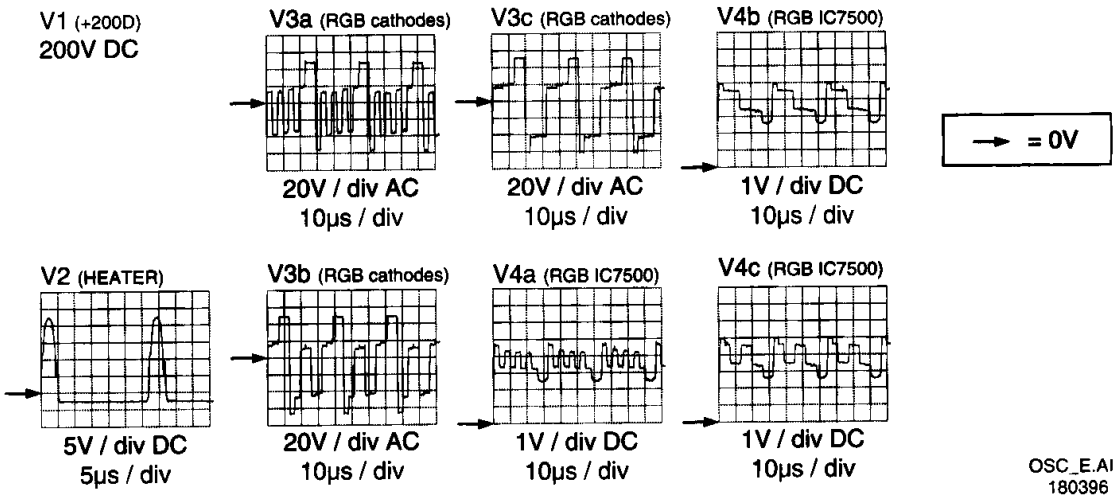

CRT+SCAVEM PANEL
FROM SSP
S40
FROM LOT
FROM LSP
L24
BC-INFO
EHT-INFO
GND-VC
R-VC
G-VC
B-VC
BANDWITH LIMITING
+12V
+200A
+12Vsvm
+3V
+13D
VG2
n.c.
+200D
GND-SUPPLY-DEFL
HEATER
VSCAVEM
7330
7340
7350
7338 BC858
7348 BC858
7358 BC858
7374 BF423
7377 BC848
BZX79-C15V
1N4148
BZX79-C10V

Bildröhren & SCAVEM-Platine / Platine tube-image & SCAVEM

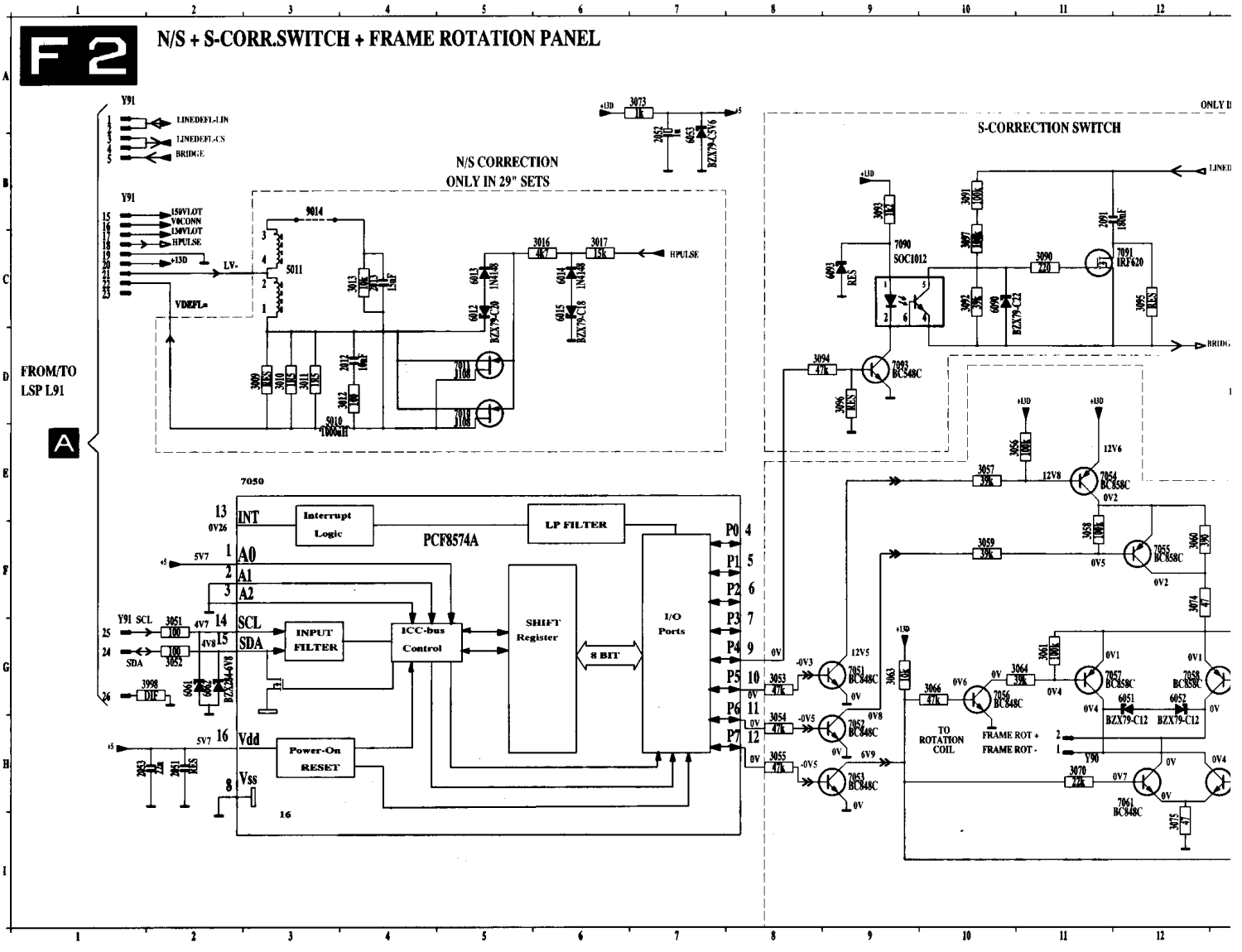


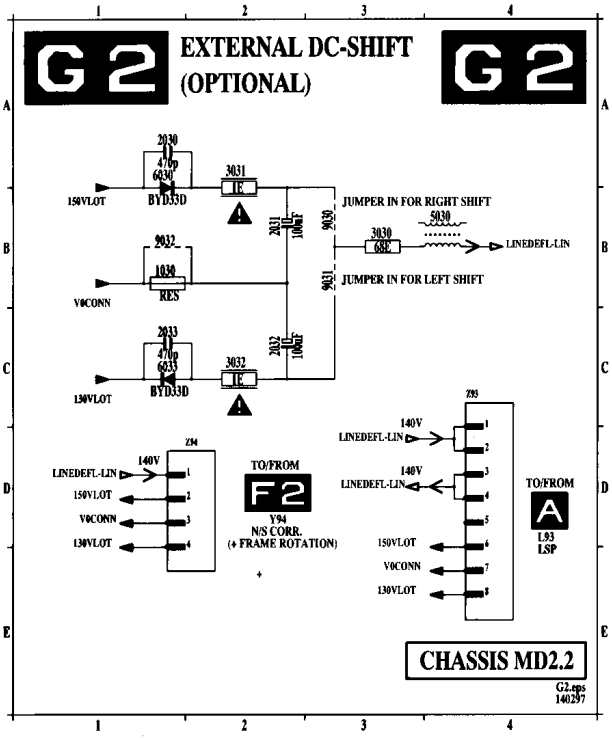
with no heatsinks

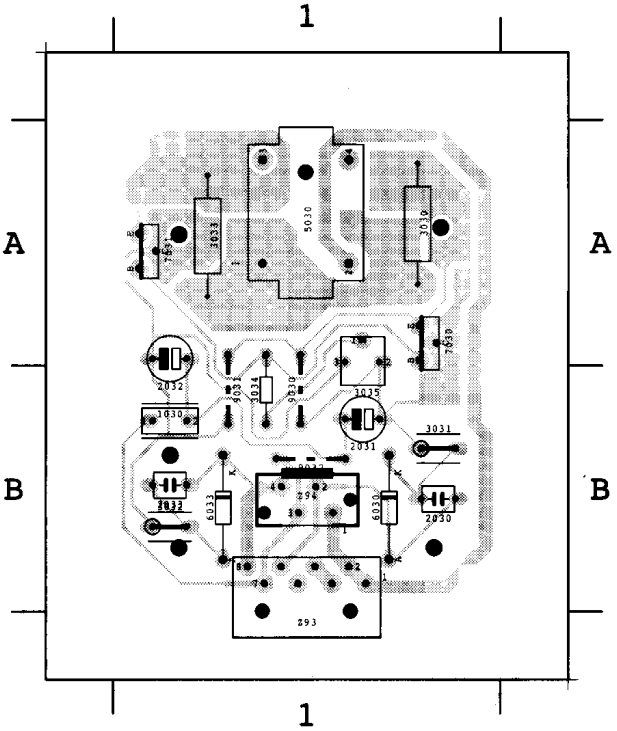
TDA6111	TDA6101
TDA6111	TDA6101
TDA6111	TDA6101
TDA6111	TDA6101
6u8	RES
6u8	RES
6u8	RES
RES	+
RES	+
RES	+
22p	15p
22p	15p
22p	15p
8p2	15p
6p8	12p
6p8	12p
3n3	1n
3n3	1n
3n3	1n
0E	33E
0E	33E
0E	33E


V1 (+200D)
200V DC
V3a (RGB cathodes)
20V / div AC
10µs / div
V3c (RGB cathodes)
20V / div AC
10µs / div
V4b (RGB IC7500)
1V / div DC
10µs / div
= 0V
V2 (HEATER)
5V / div DC
5µs / div
V3b (RGB cathodes)
20V / div AC
10µs / div
V4a (RGB IC7500)
1V / div DC
10µs / div
V4c (RGB IC7500)
1V / div DC
10µs / div
OSC_E.AI
180396

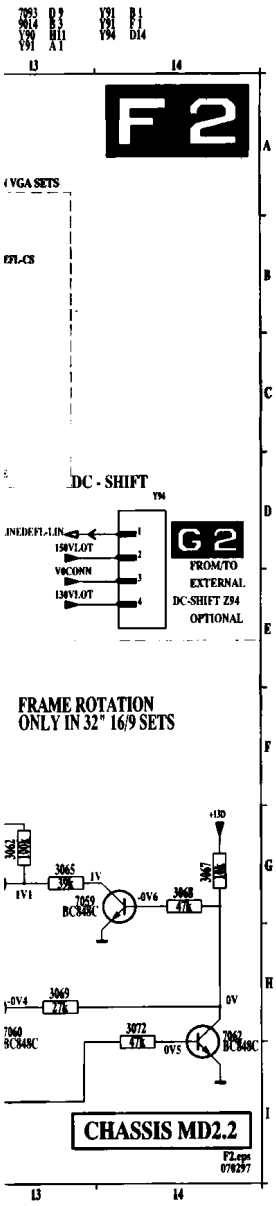
North/South + Frame rotation + S-correction panel / Nord/Süd + Drehrahmen + S-Korrekturplatine / Platine N/S + rotation de Trame + Correction S



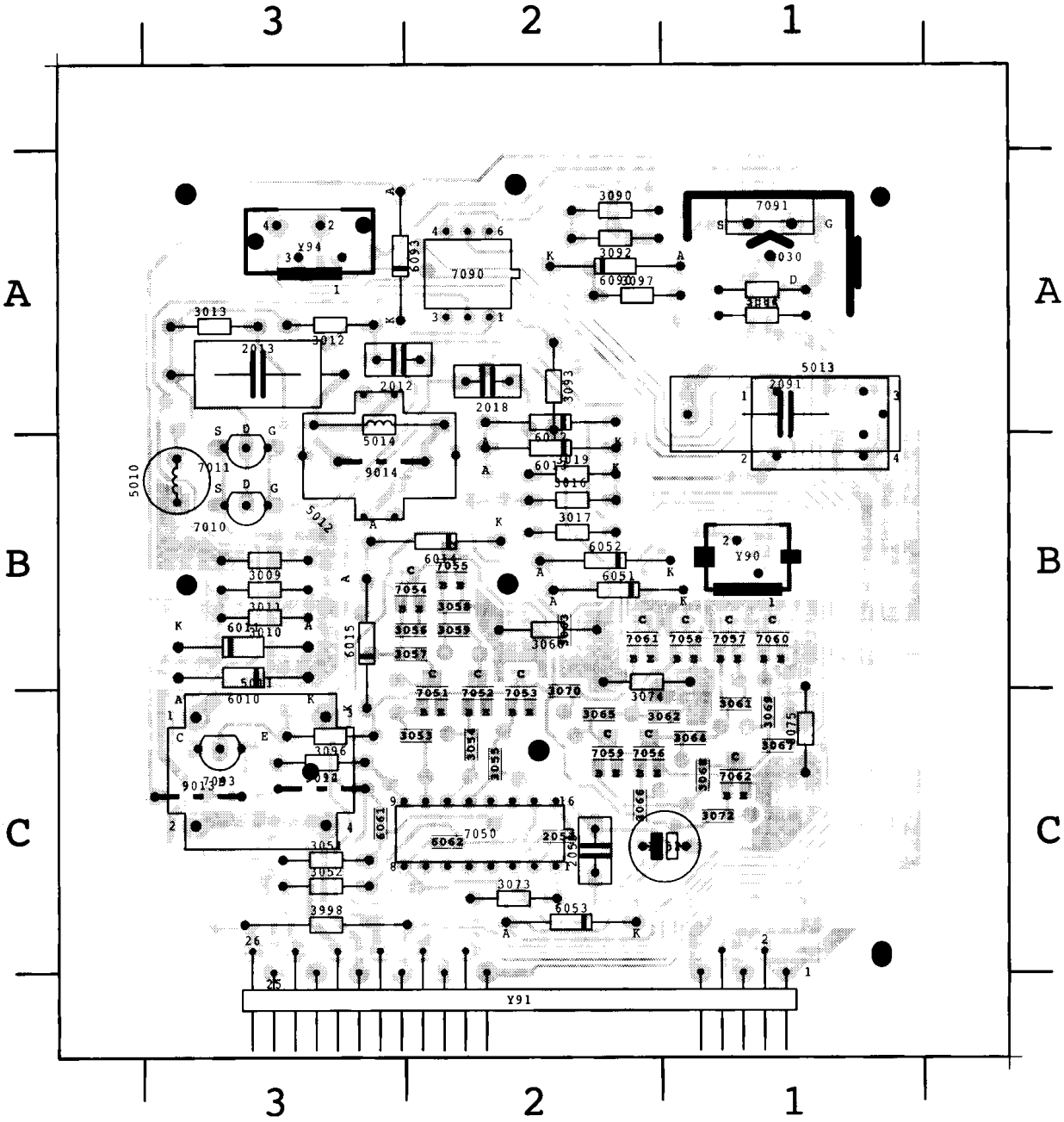




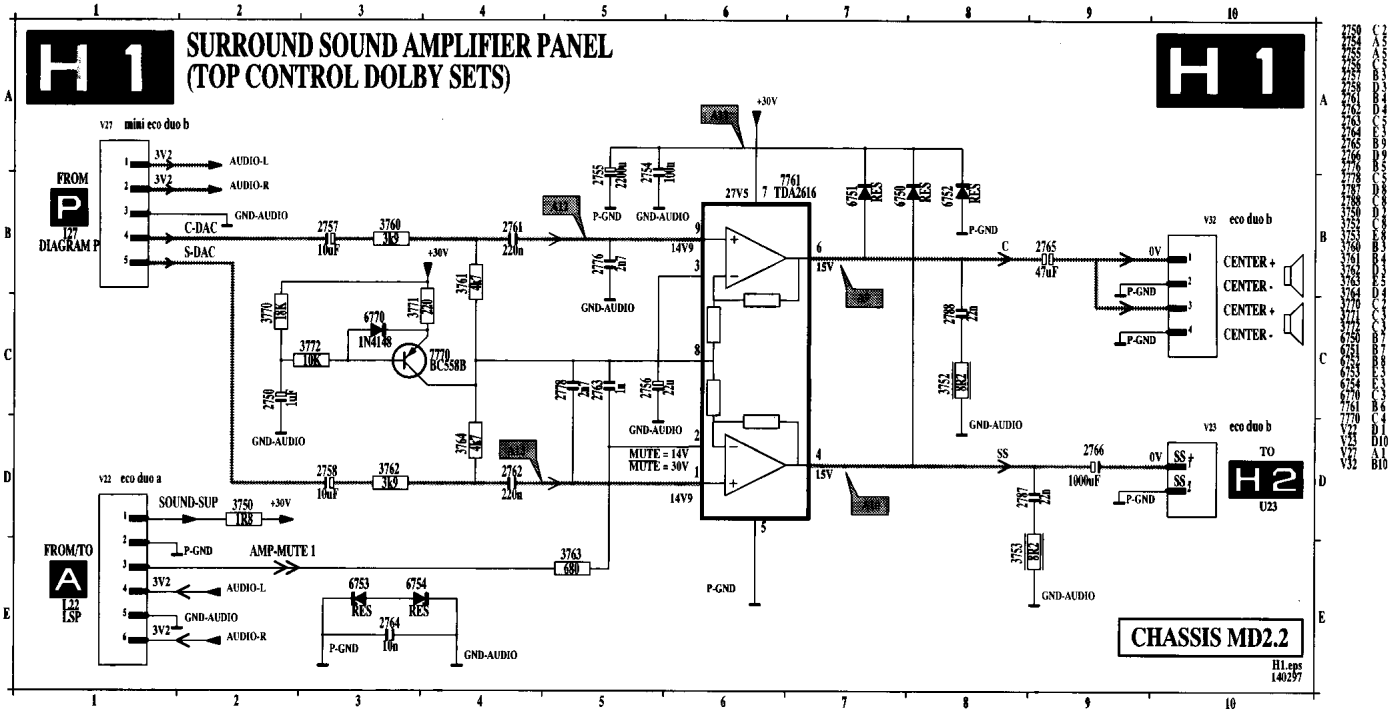
External DC shift panel /
Externe-DC-verschiebungs-Platine / Platine déphasage externe CC



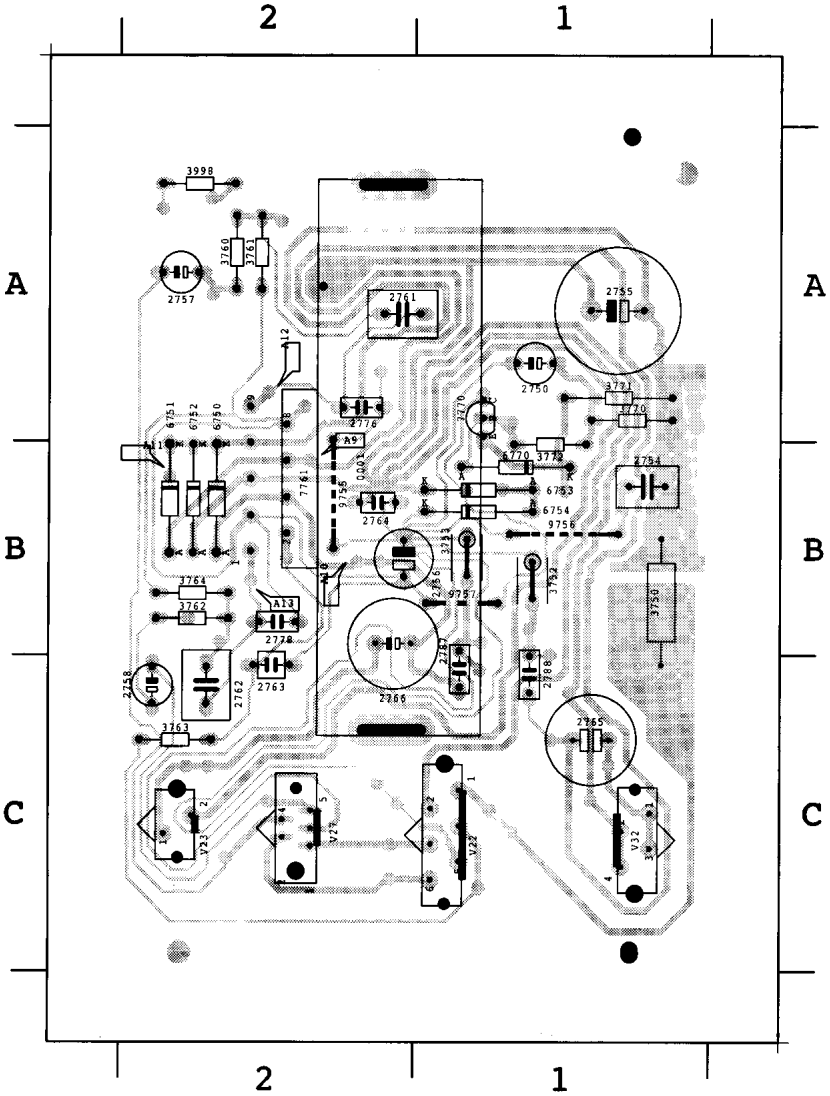
0030 A 1	3010 B 3	3053 C 2	3062 C 1	3072 C 1	3095 A 1	6010 B 3	6061 C 3	7053 C 2	7062 C 1	Y94 A 3
2012 A 2	3011 B 3	3054 C 2	3063 B 2	3073 C 2	3096 C 3	6011 B 3	6062 C 2	7054 B 2	7090 A 2	
2013 A 3	3012 A 3	3055 C 2	3064 C 1	3074 B 1	3097 A 2	6012 A 2	6090 A 1	7055 B 2	7091 A 1	
2018 A 2	3013 A 3	3056 B 2	3065 C 2	3075 C 1	3998 C 3	6013 B 2	6093 A 3	7056 C 2	7093 C 3	
2051 C 2	3016 B 2	3057 B 2	3066 C 2	3090 A 2	5010 B 3	6014 B 3	7010 B 3	7057 B 1	9012 C 3	
2052 C 1	3017 B 2	3058 B 2	3067 C 1	3091 A 1	5011 C 3	6015 B 3	7011 B 3	7058 B 1	9013 C 3	
2053 C 2	3019 B 2	3059 B 2	3068 C 1	3092 A 2	5012 A 3	6051 B 2	7050 C 2	7059 C 2	9014 B 2	
2091 A 1	3051 C 3	3060 B 2	3069 C 1	3093 A 2	5013 A 1	6052 B 2	7051 C 2	7060 B 1	Y90 B 1	
3009 B 3	3052 C 3	3061 C 1	3070 C 2	3094 C 3	5014 A 2	6053 C 2	7052 C 2	7061 B 2	Y91 C 1	

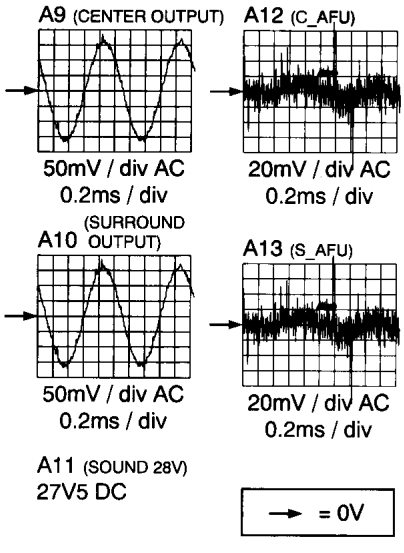


Surround sound panel / Surround Sound-Platine / Platine son Surround



0001 A 2 2757 A 2 2764 B 2 2787 B 1 3760 A 2 3770 A 1 6751 B 2 7761 B 2 V22 C 1
2750 A 1 2758 C 2 2765 C 1 2788 C 1 3761 A 2 3771 A 1 6752 B 2 7770 A 1 V23 C 2
2754 B 1 2761 A 2 2766 B 2 3750 C 1 3762 B 2 3772 B 1 6753 B 1 9755 B 2 V27 C 2
2755 A 1 2762 C 2 2776 A 2 3752 B 1 3763 C 2 3998 A 2 6754 B 1 9756 B 1 V32 C 1
2756 B 2 2763 C 2 2778 B 2 3753 B 1 3764 B 2 6750 B 2 6770 B 1 9757 B 1





OSC_H1.AI
130396

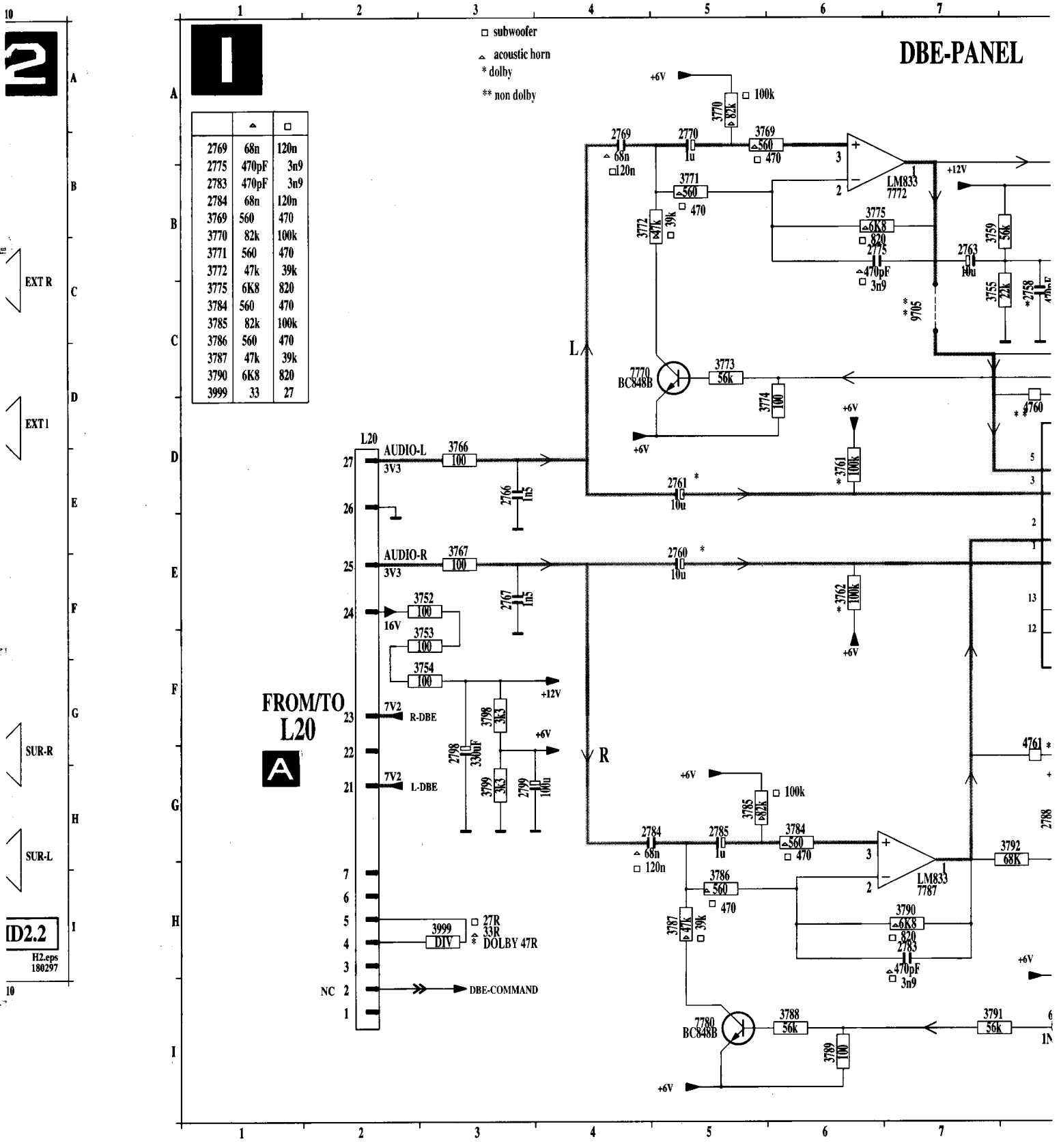
Clickfit panel / Clickfit-Platine / Platine borne de raccordement

2702 D7	2705 C8	2708 H8	3702 D4	3998 B5	5703 G9	6702 E8	9702 E4	9705 E6	CF2 B10	U23 H3	U37 F7	V2 D9	V5 D9
2703 E6	2706 D8	2709* H7	3703 H4	5701 C9	5704 H9	6703 H7	9703 E5	9706 F6	SK1 B3	U26 A2	U38 C2	V3 G9	
2704 F6	2707 G8	3701 C5	3704* H5	5702 D9	6701 C8	9701 E4	9704 E5	9712 H8	U138 G3	U36 E7	V1 C9	V4 H9	

1 2 3 4 5 6 7 8 9

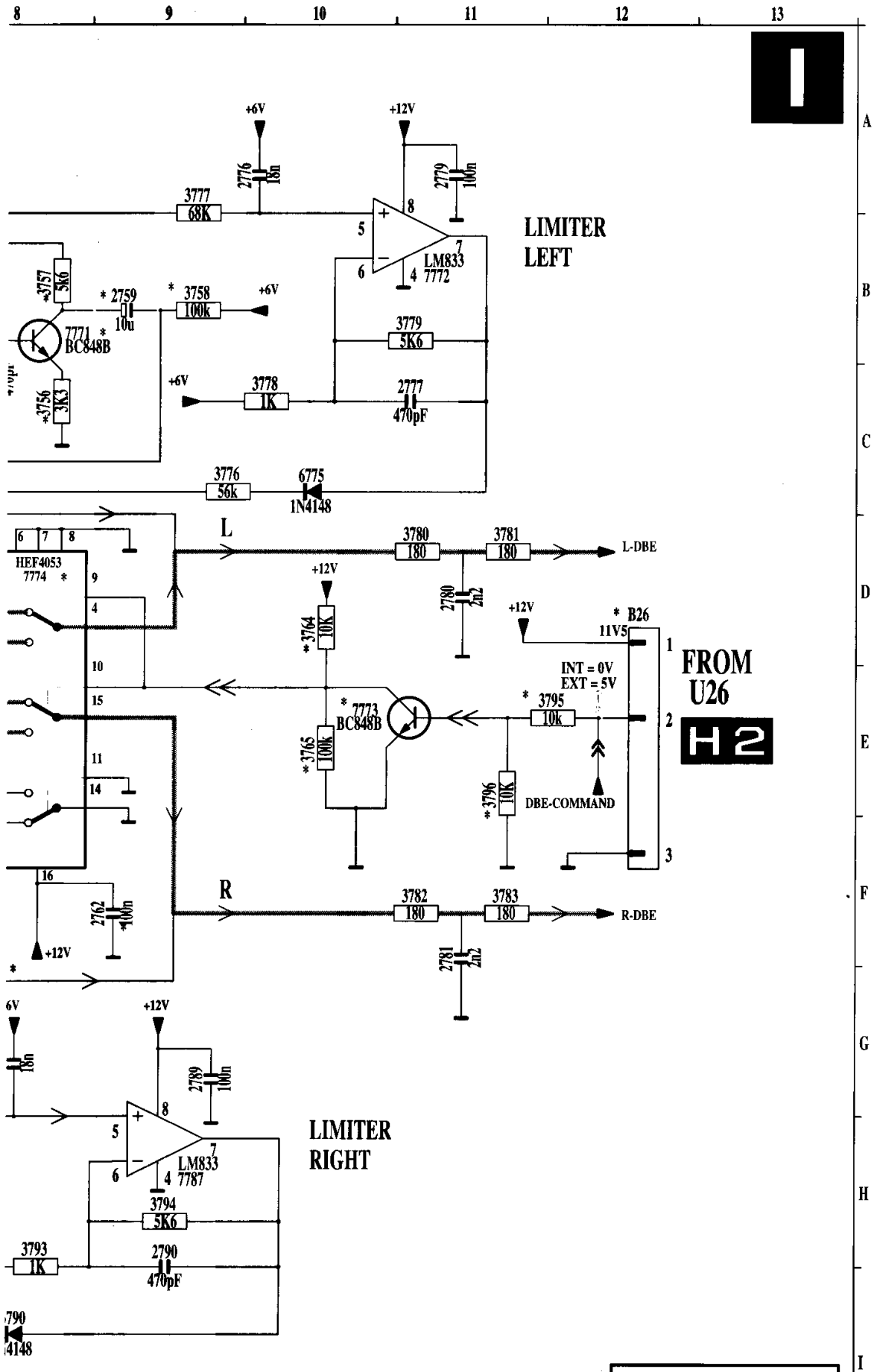
H2 CLICKFIT - PANEL (DOLBY SETS ONLY) H1

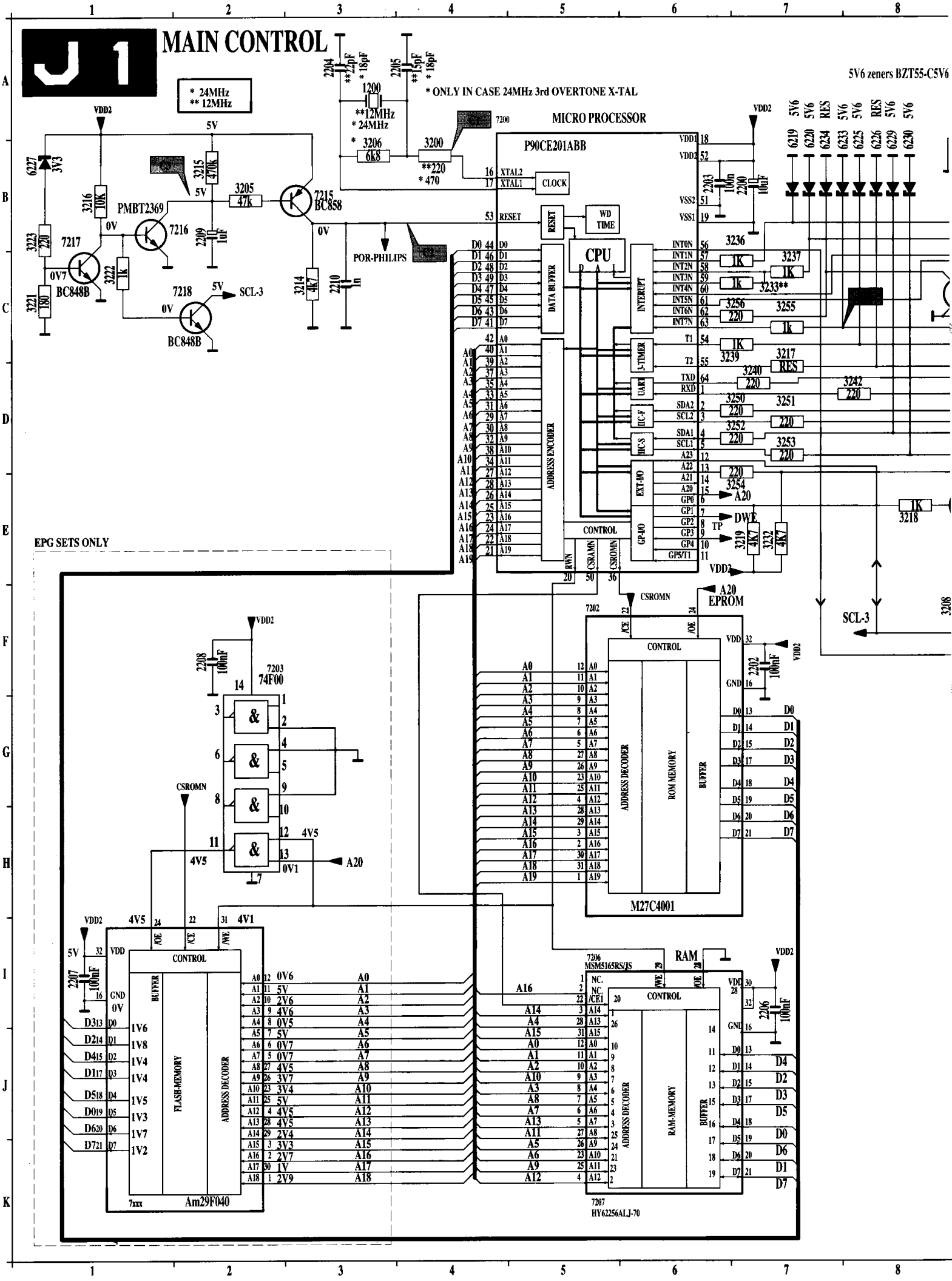
DBE (Dynamic Bass Enhancement) panel / DBE Dynamic Bass Enhancement)-Platine



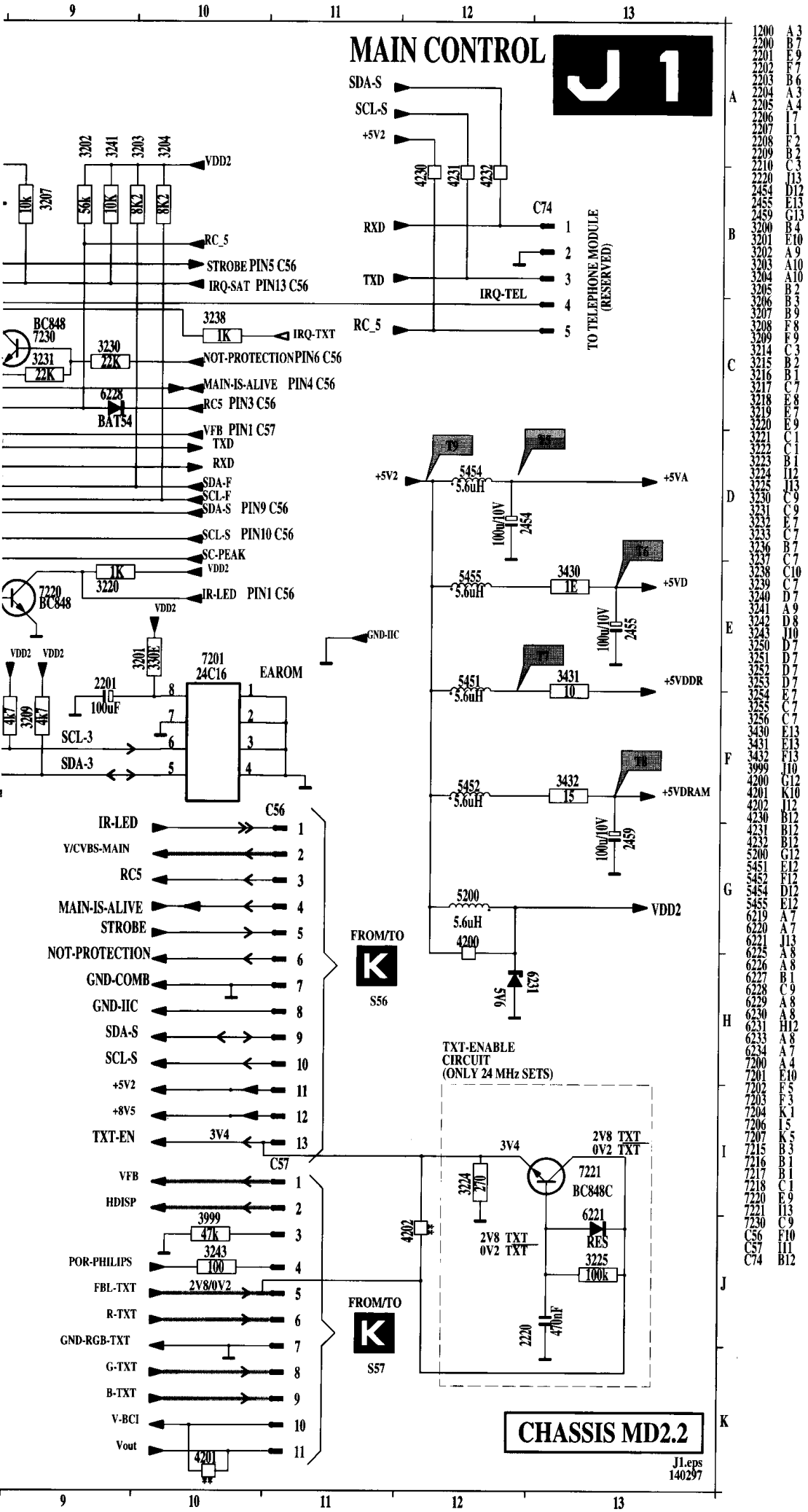
	△	□
2769	68n	120n
2775	470pF	3n9
2783	470pF	3n9
2784	68n	120n
3769	560	470
3770	82k	100k
3771	560	470
3772	47k	39k
3775	6K8	820
3784	560	470
3785	82k	100k
3786	560	470
3787	47k	39k
3790	6K8	820
3999	33	27

Platine DBE (Amélioration Dynamique des Basses




J 1
MAIN CONTROL
* 24MHz
** 12MHz
* ONLY IN CASE 24MHz 3rd OVERTONE X-TAL
5V6 zeners BZT55-C5V6
MICRO PROCESSOR
P90CE201ABB
CLOCK
RESET
WD TIME
CPU
DATA BUFFER
ADDRESS ENCODER
INTERUPT
3-TIMER
UART
IIC-F
IMCS
EXT-I/O
GP-I/O
CONTROL
POR-PHILIPS
SCL-3
EPG SETS ONLY
74F00
CSROMN
A20
EPROM
M27C4001
ADDRESS DECODER
ROM MEMORY
BUFFER
RAM
MSM5165RS/JS
HY62256ALJ-70
RAM-MEMORY
FLASH-MEMORY
Am29F040
DWE
TP

MAIN CONTROL J 1



CHASSIS MD2.2

J1.eps 140297

1200	A 3	
2200	B 7	
2201	E 9	
2202	F 7	
2203	B 6	
2204	A 3	
2205	A 4	
2206	I 7	
2207	I 1	
2208	F 2	
2209	B 2	
2210	C 3	
2220	J 13	
2454	D 12	
2455	E 13	
2459	G 13	
3200	B 4	
3201	E 10	
3202	A 9	
3203	A 10	
3204	A 10	
3205	B 2	
3206	B 3	
3207	B 9	
3208	F 8	
3209	F 9	
3214	C 3	
3215	B 2	
3216	B 1	
3217	C 7	
3218	E 8	
3219	E 7	
3220	E 9	
3221	C 1	
3222	C 1	
3223	B 1	
3224	I 12	
3225	J 13	
3230	C 9	
3231	C 9	
3232	E 7	
3233	C 7	
3236	B 7	
3237	C 7	
3238	C 10	
3239	C 7	
3240	D 7	
3241	A 9	
3242	D 8	
3243	J 10	
3250	D 7	
3251	D 7	
3252	D 7	
3253	D 7	
3254	E 7	
3255	C 7	
3256	C 7	
3430	E 13	
3431	E 13	
3432	F 13	
3999	J 10	
4200	G 12	
4201	K 10	
4202	J 12	
4230	B 12	
4231	B 12	
4232	B 12	
5200	G 12	
5451	E 12	
5452	F 12	
5454	D 12	
5455	E 12	
6219	A 7	
6220	A 7	
6221	J 13	
6225	A 8	
6226	A 8	
6227	B 1	
6228	C 9	
6229	A 8	
6230	A 8	
6231	H 12	
6233	A 8	
6234	A 7	
7200	A 4	
7201	E 10	
7202	F 5	
7203	F 3	
7204	K 1	
7206	I 5	
7207	K 5	
7215	B 3	
7216	B 1	
7217	B 1	
7218	C 1	
7220	E 9	
7221	I 13	
7230	C 9	
C56	F 10	
C57	I 11	
C74	B 12	

C1 (CLOCK)
0.5V / div DC
0.2ms / div

T2c (B_TXT)
0.2V / div DC
10µs / div

C2 OFF-ON(PORP)
1V / div DC
50ms / div

T3 (CVBS)
0.2V / div AC
10µs / div

C2 ON-OFF(PORP)
1V / div DC
50ms / div

T4 (Y/CVBS_MAIN)
0.2V / div AC
10µs / div

C3 OFF-ON
1V / div DC
0.2s / div

T5 (+5V A) 5V DC
T6 (+5V D) 5V DC
T7 (+5V DDR) 5V DC
T8 (+5V DRAM) 5V DC

C3 ON-OFF
1V / div DC
0.2s / div

T9 (+5V2) 5V DC

C4 (MAIN IS ALIVE) see § 6.5.1
1V / div DC
0.1s / div

T16 (VD)
1V / div DC
5ms / div

T1 (FBL_TXT)
TXT = 2V2 DC
NO TXT = 0V DC

T17 (IRQ_TXT)
2V / div DC
10ms / div

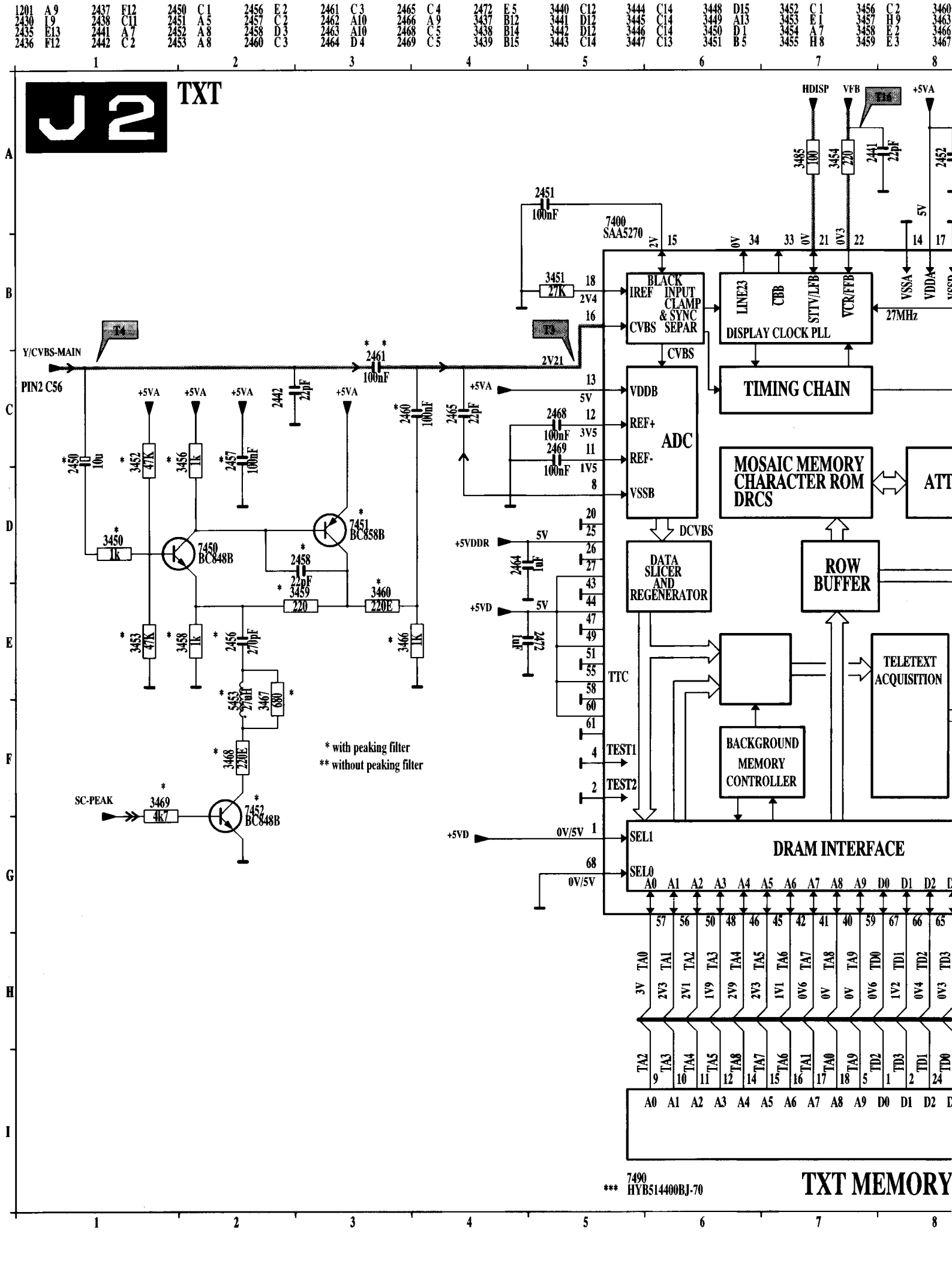
T2a (R_TXT)
0.2V / div DC
10µs / div

→ = 0V

T2b (G_TXT)
0.2V / div DC
10µs / div

OSC_J1-2.AI 250297

TXT & Control panel (TXT part) /



TXT & Control-Platine / Platine TXT & Commande

E 3	3468	F 2	3483	G12	3489	F11	3495*	F12	7400	A 5	7452	F 2	7456	C14	7490	I 5			
A10	3469	F 1	3484	G12	3490	F11	3497	B11	7449	D13	7453	D12	7457	B12					
E 3	3481	H10	3485	A 7	3491*	E12	5453	E 2	7450	D 2	7454	D14	7458	B14					
E 2	3482	H10	3488	F11	3493*	E12	5460	A10	7451	D 3	7455	C13	7459	A15					

TXT J2

BLENDING CIRCUITRY (24MHz SETS ONLY)

CRYSTAL OSCILLATOR

TXT PROCESSOR

RIBUTE LOGIC

CURSOR AND SHODOWING

CLUT

DAC

PACKET 26 PROCESSING

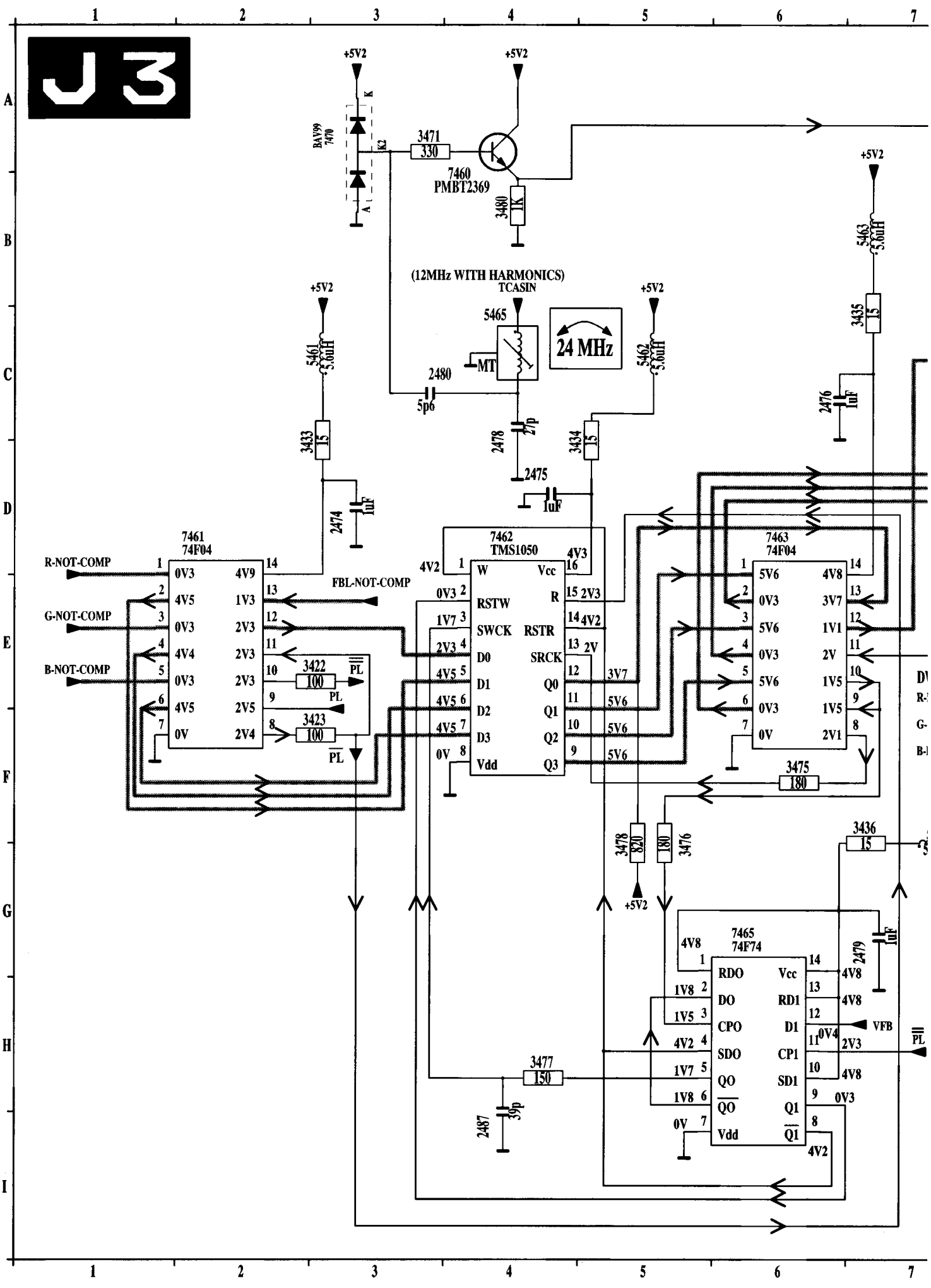
LEVEL 1 PAGE CONVERSION

I²C

* TEXT DUALSCREEN
** NO TEXT DUALSCREEN

CHASSIS MD2.2

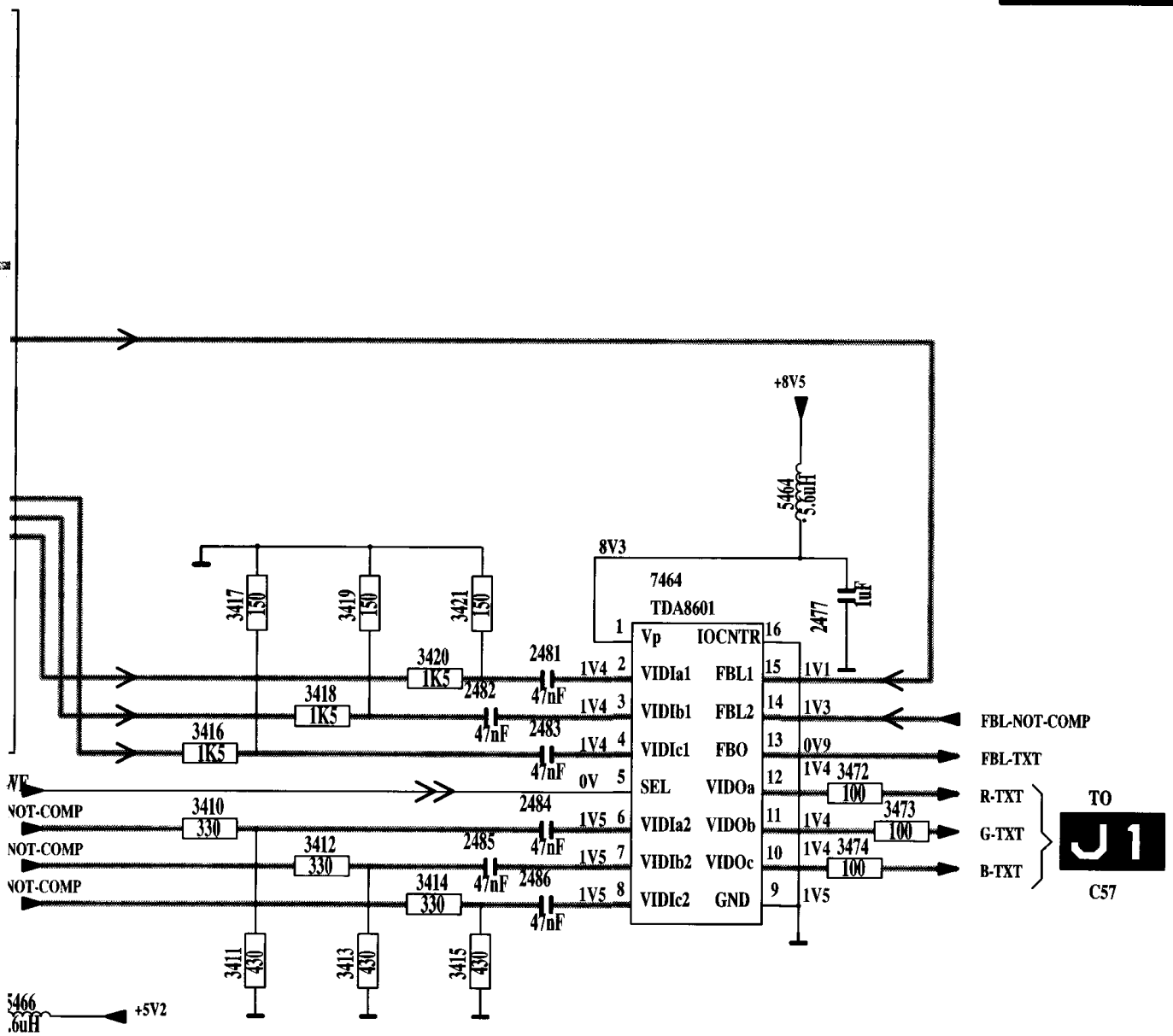
J2.eps
180297


J3
+5V2
BAV99
7470
3471
330
7460
PMBT2369
3480
1K
(12MHz WITH HARMONICS)
TCASIN
5465
MT
24 MHz
2480
5p6
2478
27p
2475
1uF
5461
5.6uH
5462
5.6uH
5463
5.6uH
3433
15
3434
15
3435
15
2474
1uF
2476
1uF
7461
74F04
R-NOT-COMP
G-NOT-COMP
B-NOT-COMP
FBL-NOT-COMP
3422
100
3423
100
PL
7462
TMS1050
W
RSTW
SWCK
D0
D1
D2
D3
Vdd
Vcc
R
RSTR
SRCK
Q0
Q1
Q2
Q3
7463
74F04
3475
180
3478
820
180
3476
3436
15
7465
74F74
RDO
DO
CPO
SDO
QO
Vdd
RD1
D1
CP1
SD1
Q1
Q1
VFB
3477
150
2487
39p
2479
1uF

TXT & Control-Platine / Platine TXT & Commande

TEXT DUALSCREEN ONLY

J3



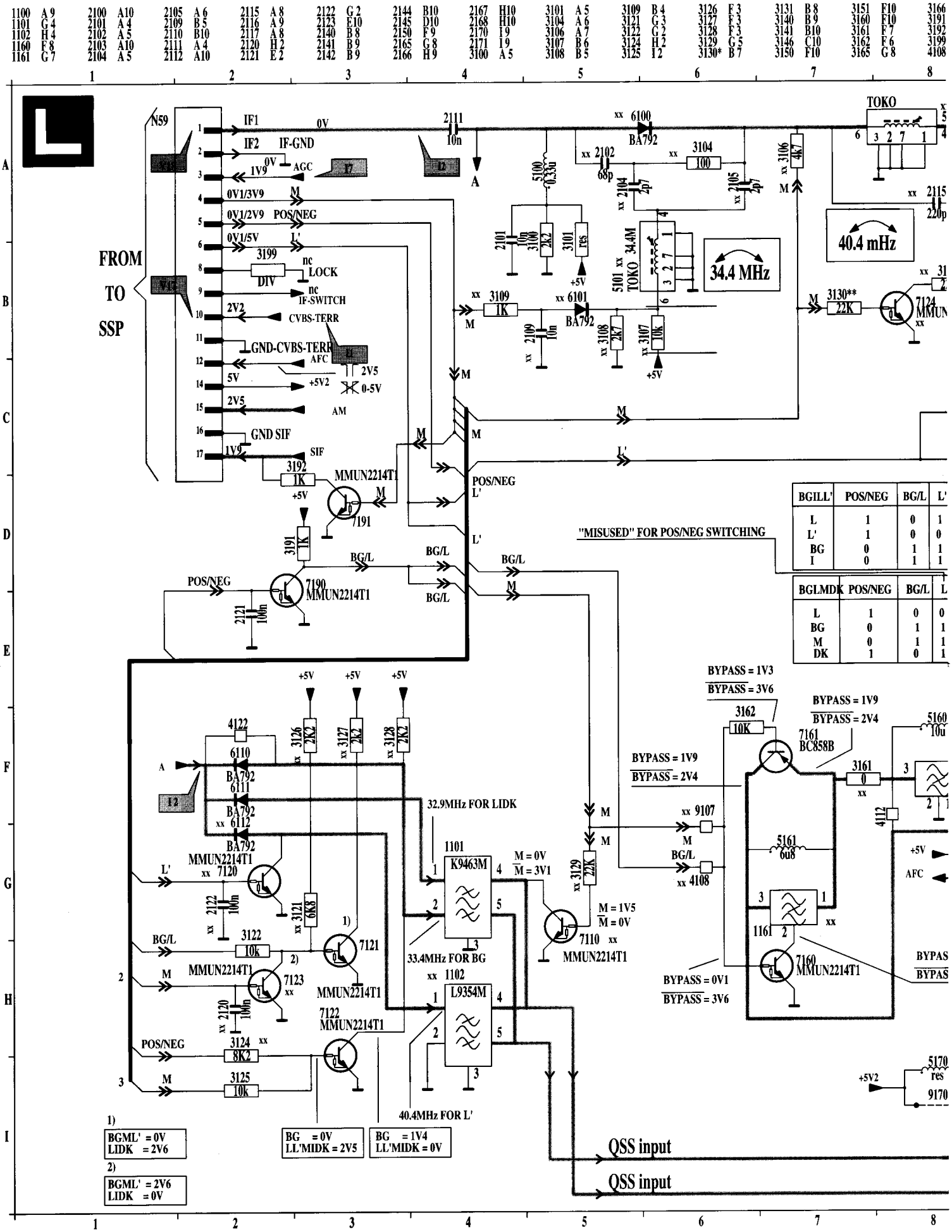
MEASURED IN TEXT DUALSCREEN MODE

CHASSIS MD2.2

J3.eps
180297

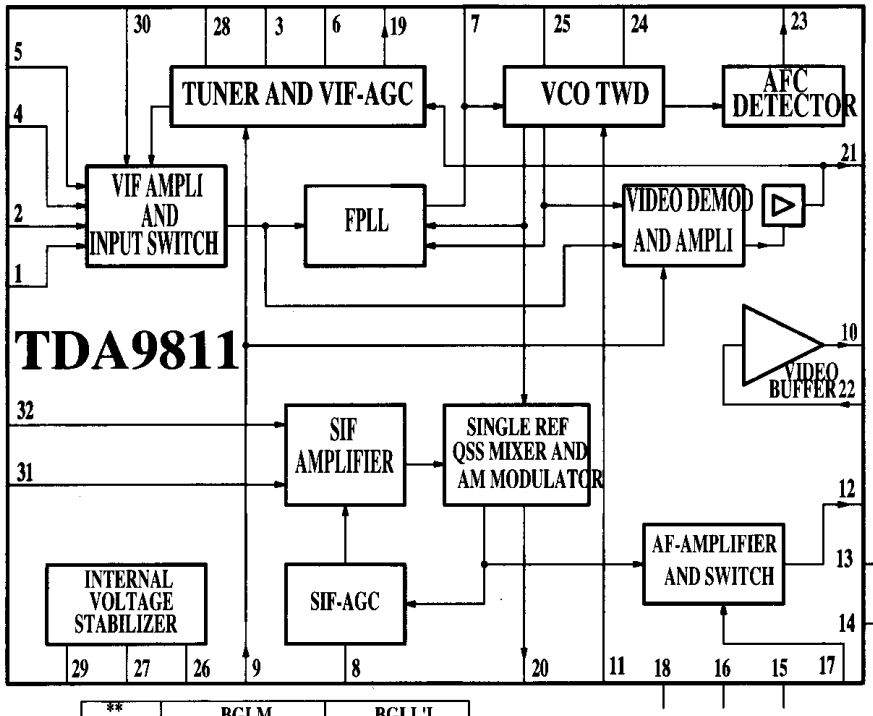
2474 D3
2475 D4
2476 C6
2477 D11
2478 C4
2479 G7
2480 C3
2481 E10
2482 E10
2483 E10
2484 E10
2485 F10
2486 F10
2487 I4
3410 E8
3411 F8
3412 F9
3413 F9
3414 F9
3415 F10
3416 E8
3417 D8
3418 E9
3419 D9
3420 E9
3421 D10
3422 E3
3423 F3
3433 C3
3434 C5
3435 C7
3436 F7
3471 A3
3472 E12
3473 E12
3474 F12
3475 F6
3476 F5
3477 H4
3478 F5
3480 B4
5461 C3
5462 C5
5463 B7
5464 D11
5465 C4
5466 F7
7460 B4
7461 D2
7462 D4
7463 D6
7464 D11
7465 G6
7470 A3

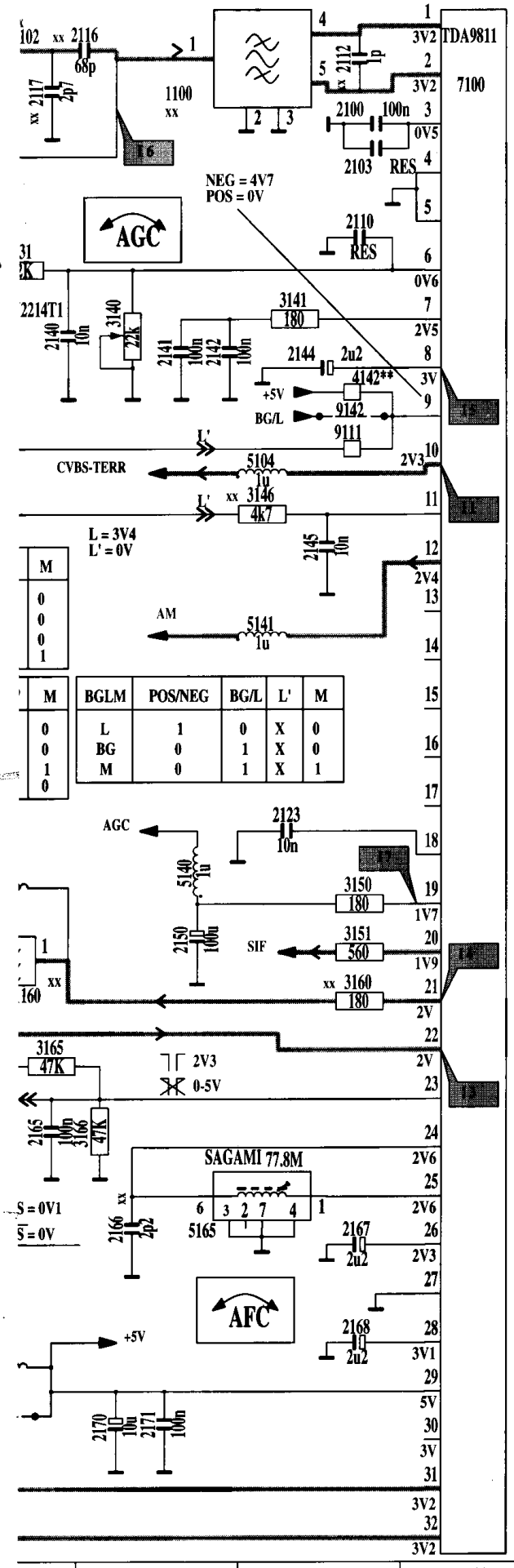
IF module / Zwischenfrequenz-Modul / Module FI



G 9	4112	F 8	5102	A 8	5161	G 7	6110	F 2	7120	G 2	7160	H 7	9111	C10
D 3	4122	F 2	5104	C10	5165	H 9	6111	F 2	7121	H 3	7161	F 7	9142	C10
C 3	4142*	C10	5140	F 9	5170	I 8	6112	G 2	7122	H 3	7190	D 3	9170	I 8
B 2	5100	A 5	5141	D10	6100	A 6	7100	A11	7123	H 2	7191	D 3	N59	A 1
G 6	5101	B 5	5160	F 8	6101	B 5	7110	H 5	7124	B 8	9107	F 6		

IF PANEL





M	BGLM	POS/NEG	BG/L	L'	M
0	L	1	0	X	0
0	BG	0	1	X	0
1	M	0	1	X	1
0					

**	BGLM	BGLL'I
1100	OFWG3956M	OFWG3953M
1102	-	OFWG9354M
1160	TPS5,5MW	TPS6,0MB
1161	TPS4,5MB	TPS5,5MW
2102	68pF	JUMPER
2104	2p7	-
2105	2p7	-
2109	10n	-
2112	-	
2115	JUMPER	330p
2116	-	56p
2117	-	2p2
2120	-	100n
2122	-	100n
3104	150	47
3106	4k7	-
3107	10K	-
3108	2k7	-
3109	1k	-
3121	-	6k8
3124	8k2	6k8
3126	-	2k2
3127	2k2	4k7
3128	2k2	4k7
3129	22k	-
3130	22k	-
3131	22k	-
3146	-	4k7
3160	180	220
4107	JUMPER	-
4108	-	4142
4142	-	-
5101	34,4MC	-
5102	-	40.4MC
6100	BA582	-
6101	BA582	-
6112	-	BA582
7110	MMUN2214T1	-
7120	-	MMUN2214T1
7123	-	MMUN2214T1
7124	MMUN2214T1	-

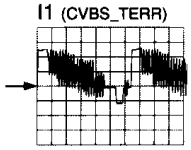
BGLMDK ; LIKE BGLM EXCEPT:	
1100	OFWG3953M
9111	IN
9142	NOT IN

CHASSIS MD2.2

L.eps
140297

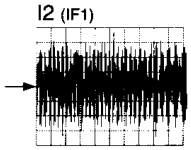
module / Zwi

I1 (CVBS_TERR)



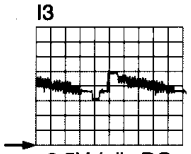
0.5V / div DC
10µs / div

I2 (IF1)



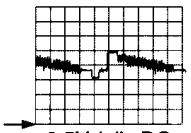
50mV / div DC
50µs / div

I3



0.5V / div DC
10µs / div

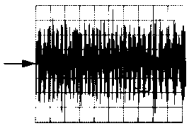
I4



0.5V / div DC
10µs / div

I5
3V DC

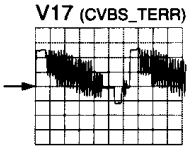
I6



50mV / div DC
50µs / div

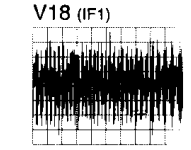
I7 (AGC)
1V9 DC

V17 (CVBS_TERR)



0.5V / div DC
10µs / div

V18 (IF1)

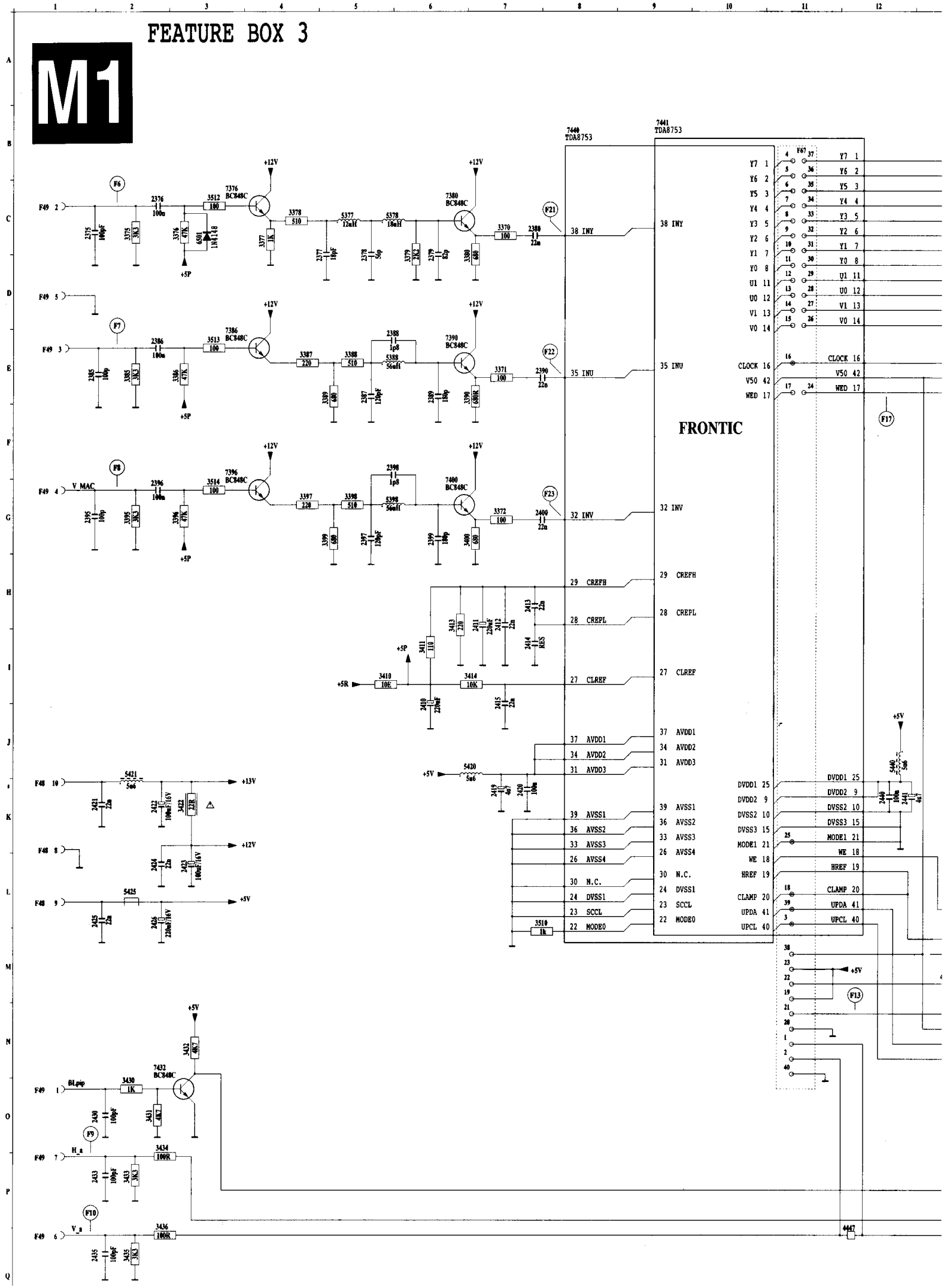


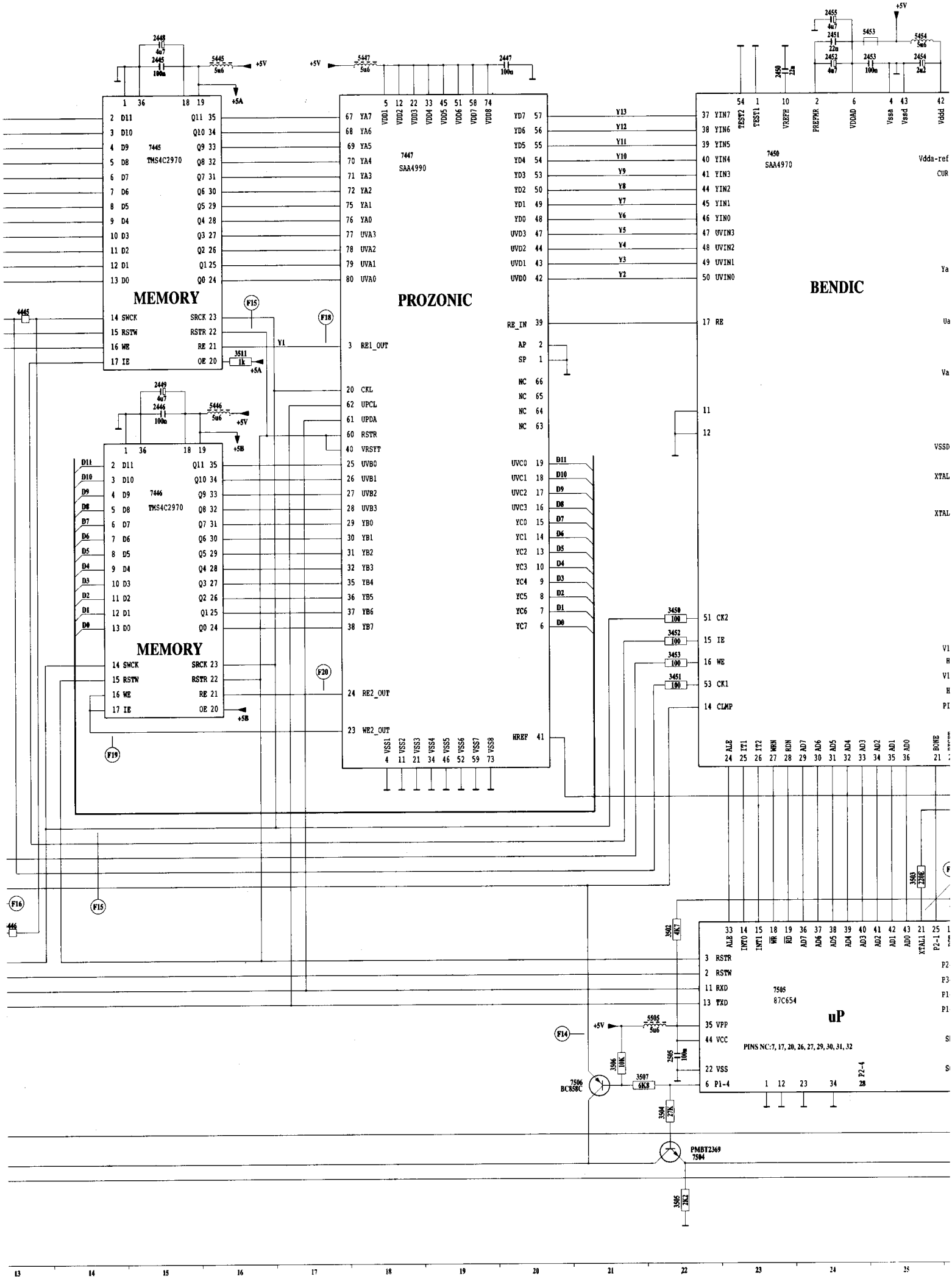
50mV / div DC
50µs / div

→ = 0V

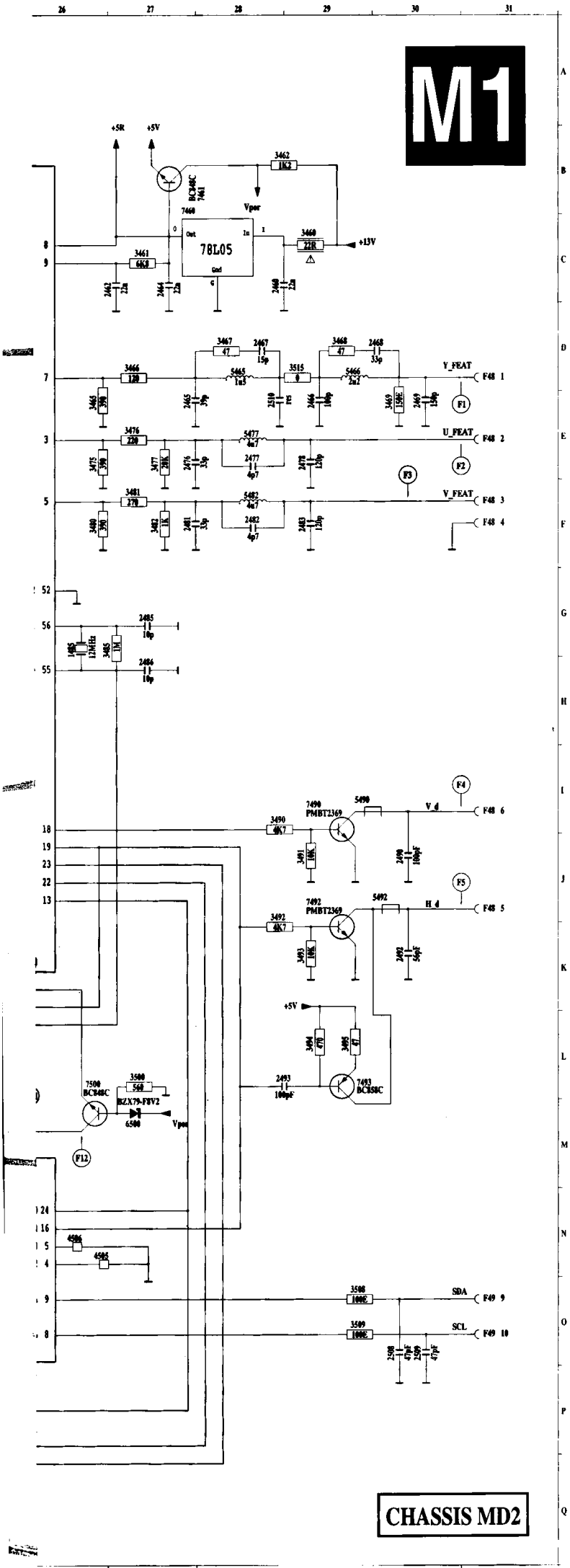
OSC_L.AI
260297

Feature Box (Digital Scan) panel /

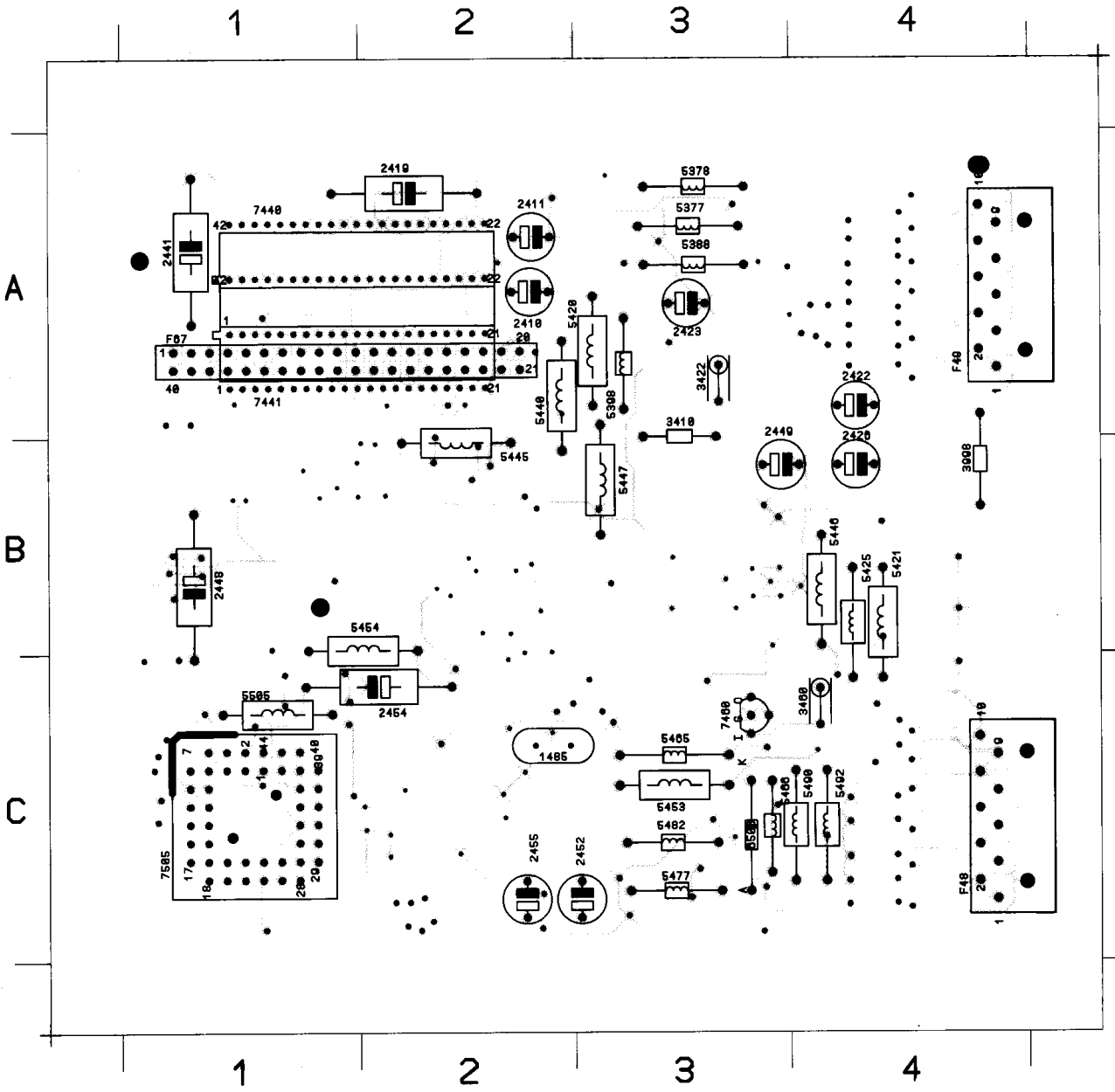



MEMORY
7445
TMS4C2970
MEMORY
7446
TMS4C2970
PROZONIC
7447
SAA4990
BENDIC
7450
SAA4970
uP
7505
87C654
PINS NC:7, 17, 20, 26, 27, 29, 30, 31, 32
7506
BC858C
PMBT2369
7504
+5V
+5A
+5B
F15
F16
F18
F19
F20
Y1

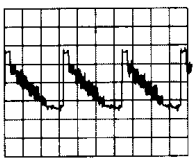
Platine Boîtier Numérique (balayage numérique)

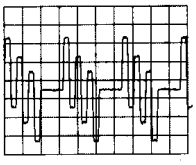


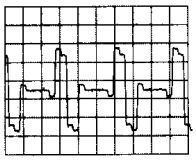
Feature Box (Digital Scan) panel /

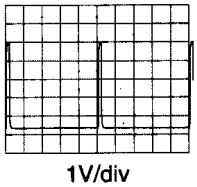


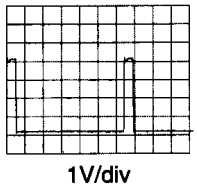
1485 C 2 2419 A 1 2426 B 4 2449 B 3 2455 C 2 3460 C 4 5378 A 3 5420 A 3 5448 B 2 5447 A 3 5465 C 3 5482 C 3 5505 C 1 7441 A 1 F48 C 4
2410 A 2 2422 A 4 2441 A 1 2452 C 3 3410 A 3 3998 B 4 5388 A 3 5421 C 4 5445 B 2 5453 C 3 5466 C 3 5490 C 4 6500 C 3 7460 C 3 F49 A 4
2411 A 2 2423 A 3 2448 B 1 2454 C 2 3422 A 3 5377 A 3 5308 A 3 5425 C 4 5448 B 4 5454 B 1 5477 C 3 5492 C 4 7440 A 1 7585 C 1 F67 A 1

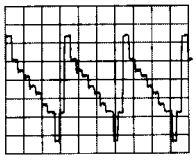
F1

100mV/div
10µs/div

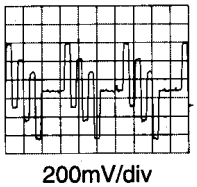
F2

200mV/div
10µs/div

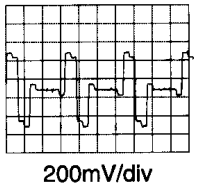
F3

200mV/div
10µs/div

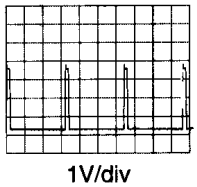
F4

1V/div
2ms/div

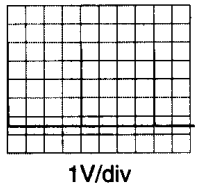
F5

1V/div
5µs/div

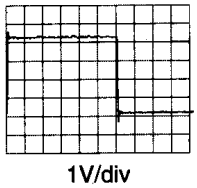
F6

200mV/div
20µs/div

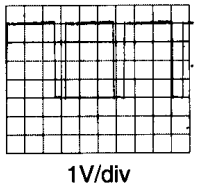
F7

200mV/div
20µs/div

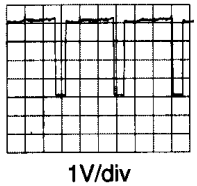
F8

200mV/div
20µs/div

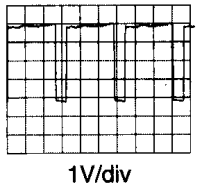
F9

1V/div
20µs/div

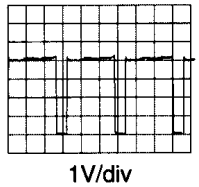
F10

1V/div
5ms/div

F16

1V/div
0.5µs/div

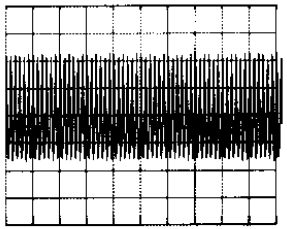
F17

1V/div
20µs/div

F18

1V/div
10µs/div

F19

1V/div
10µs/div

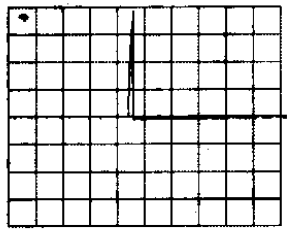
F20

1V/div
10µs/div

F11



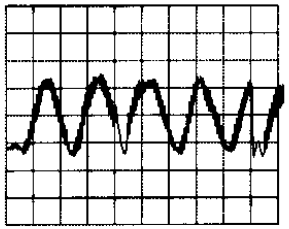
1V/div
0.5µs/div

F12



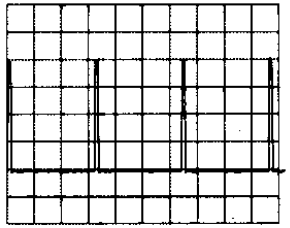
1V/div
50ms/div

F13



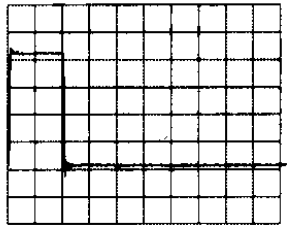
500V/div
50ns/div

F14



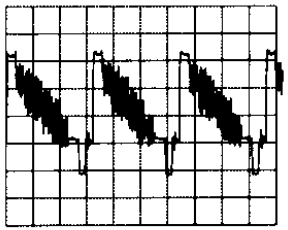
1V/div
20µs/div

F15



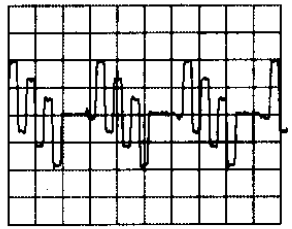
1V/div
0.5µs/div

F21



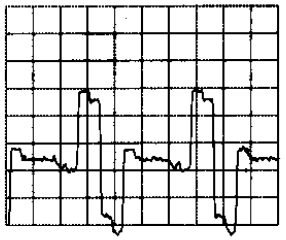
200mV/div
20µs/div

F22



200mV/div
20µs/div

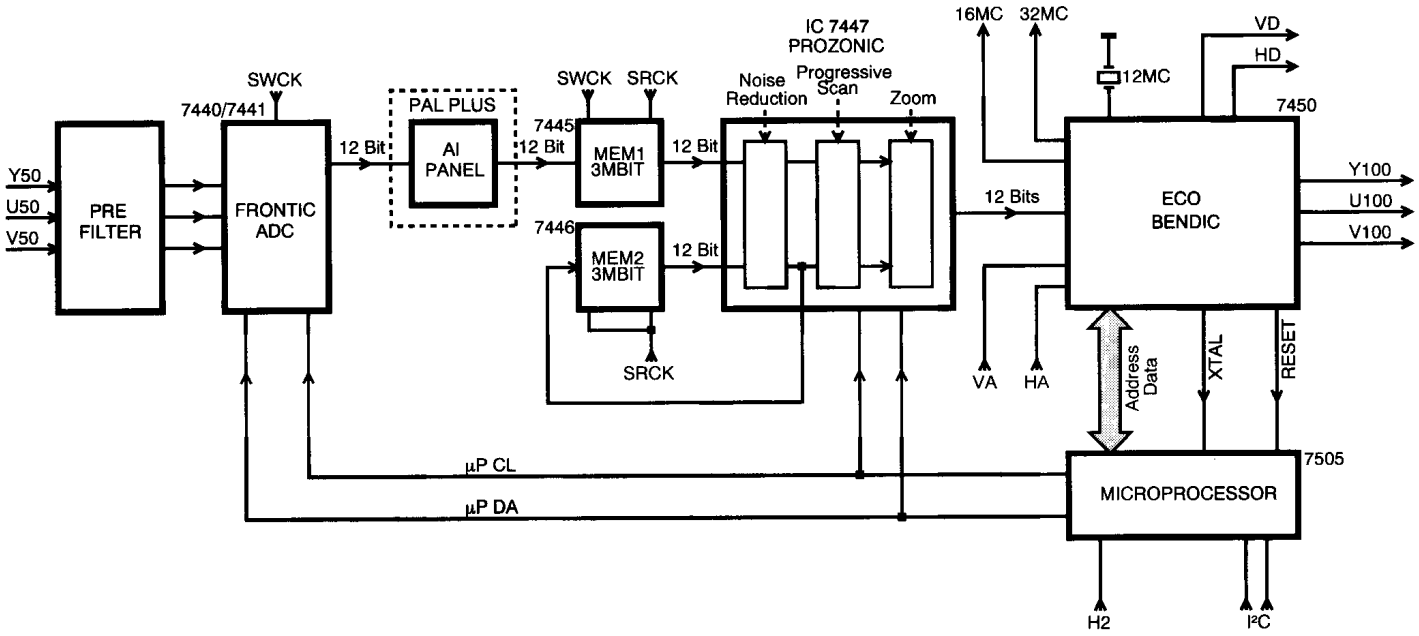
F23



200mV/div
20µs/div

PCS 91 167

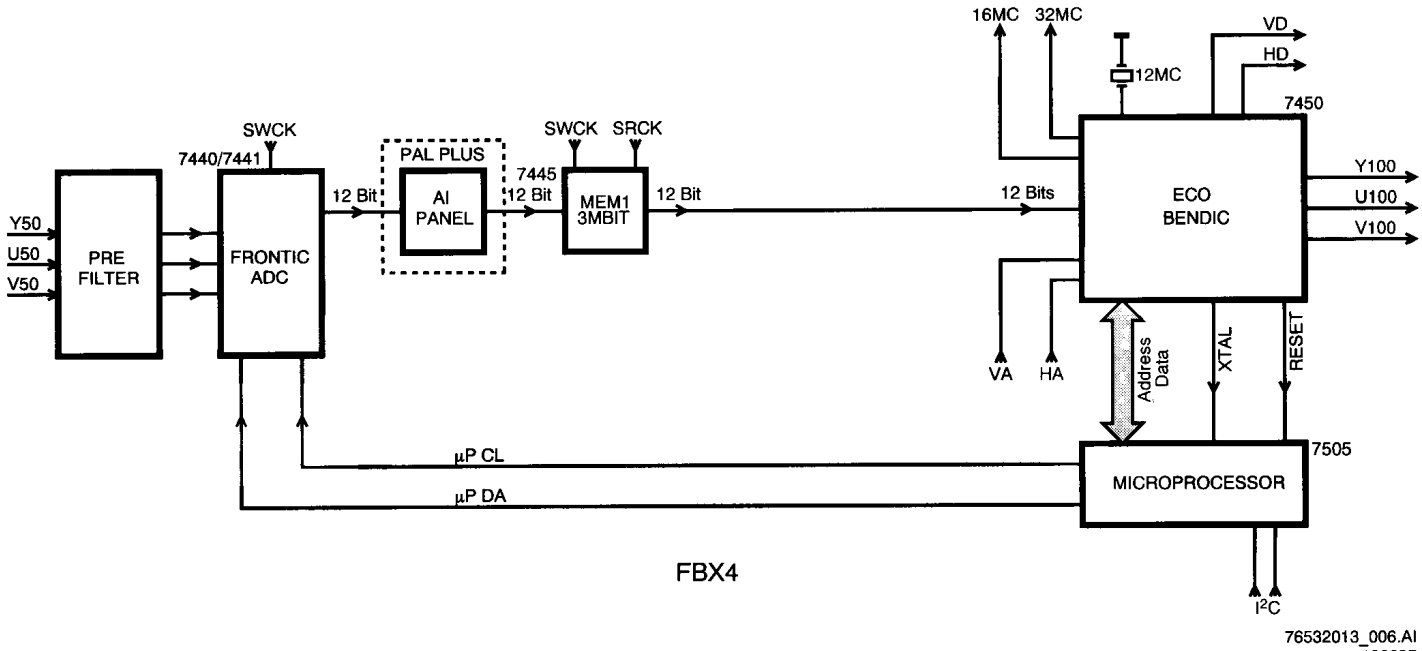
Feature box 3 (digital scan) M1



FBX3

66532024_016B.AI
080396

Feature box 4 (ECO) M2

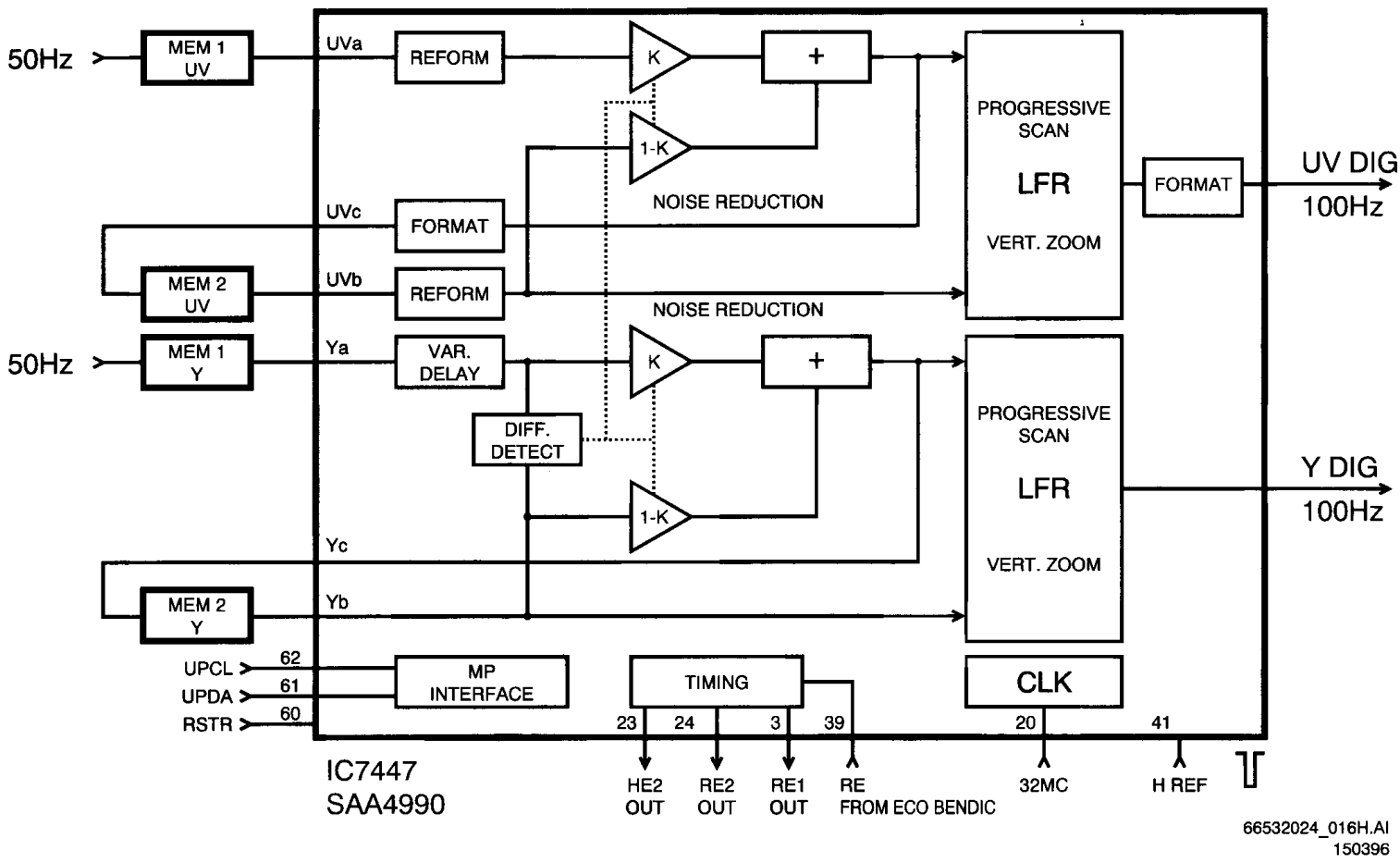


FBX4

76532013_006.AI
190297

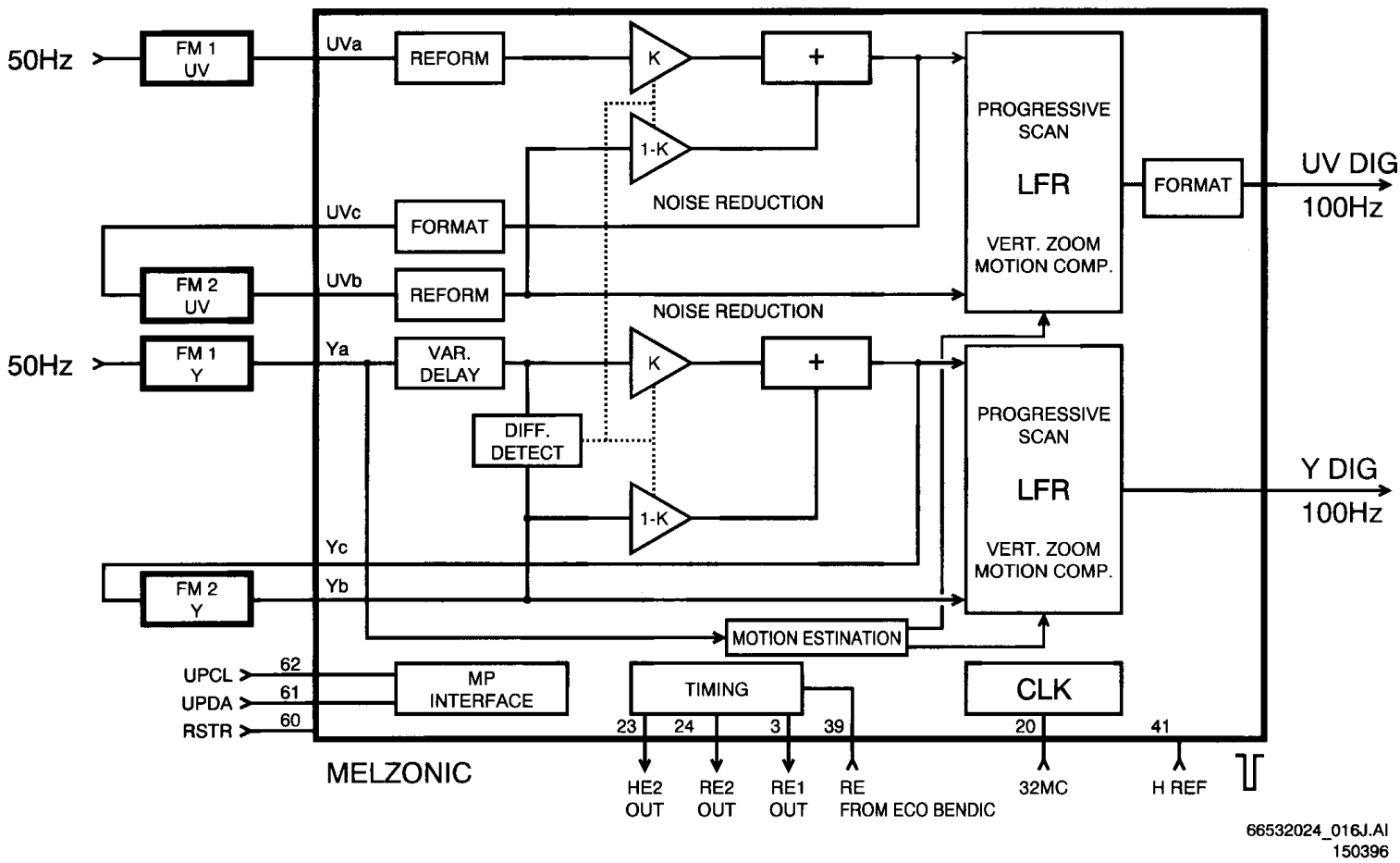
Schaltbilder der ICs in den Feature-Boxen /

Prozinic SAA 4990 (IC7447 Feature box digital scan) M1



66532024_016H.AI
150396

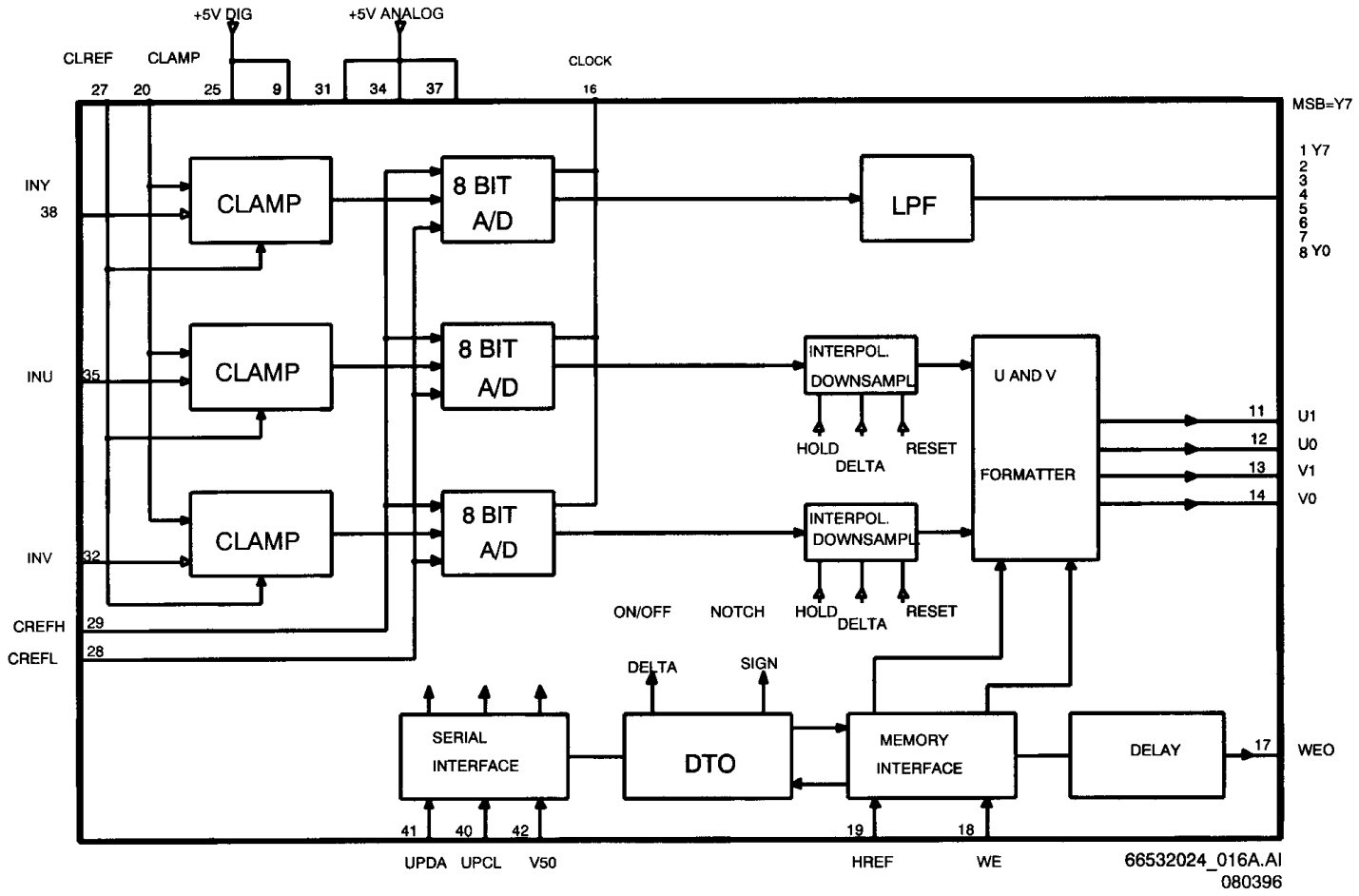
MELZONIC SAA 4991 (IC 7447 Feature box natural motion) M1



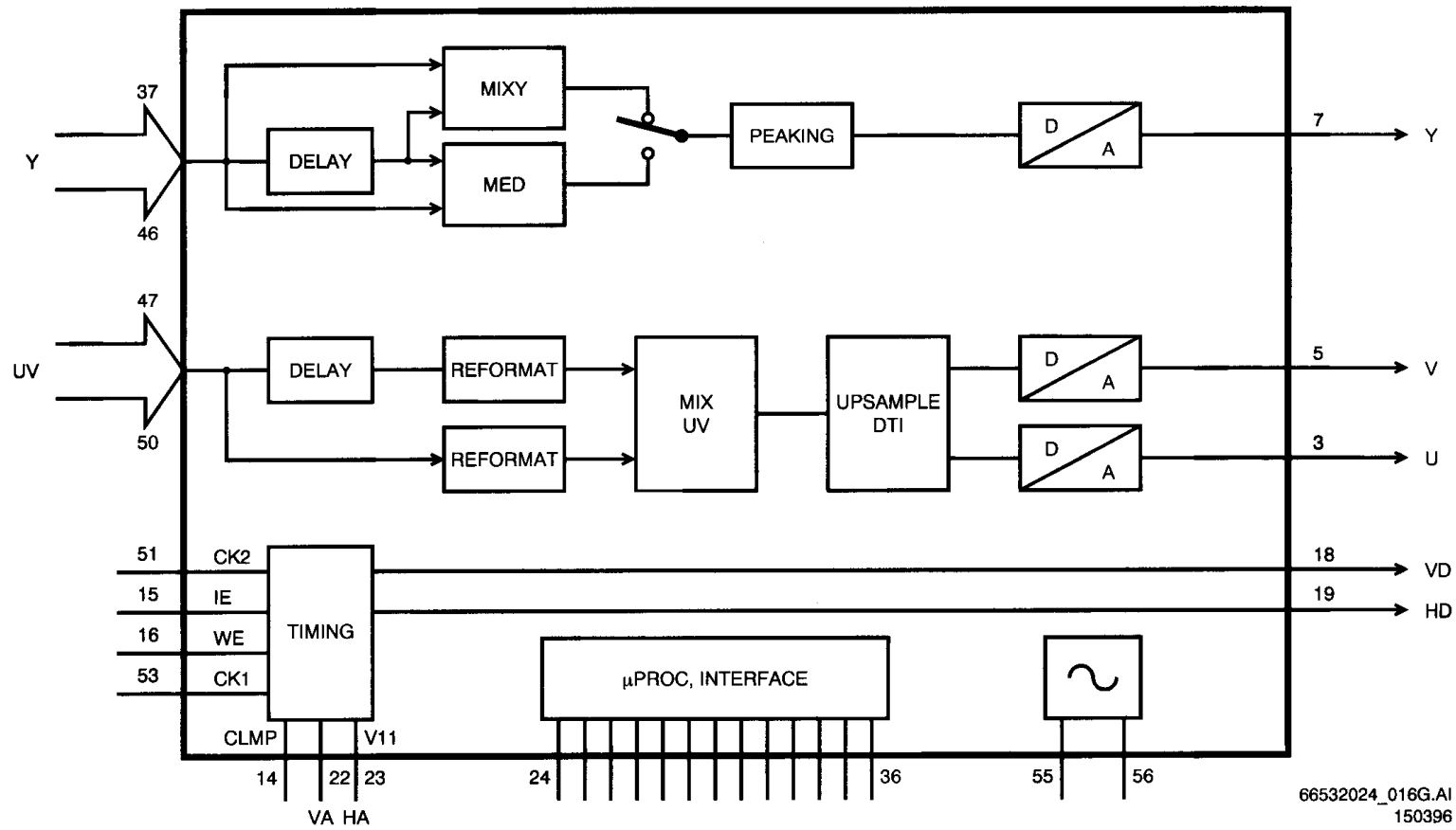
66532024_016J.AI
150396

Diagrammes synoptiques des CI

FRONTIC TDA 8753 (IC 7440/7441 in both feature boxes) M1 / M2

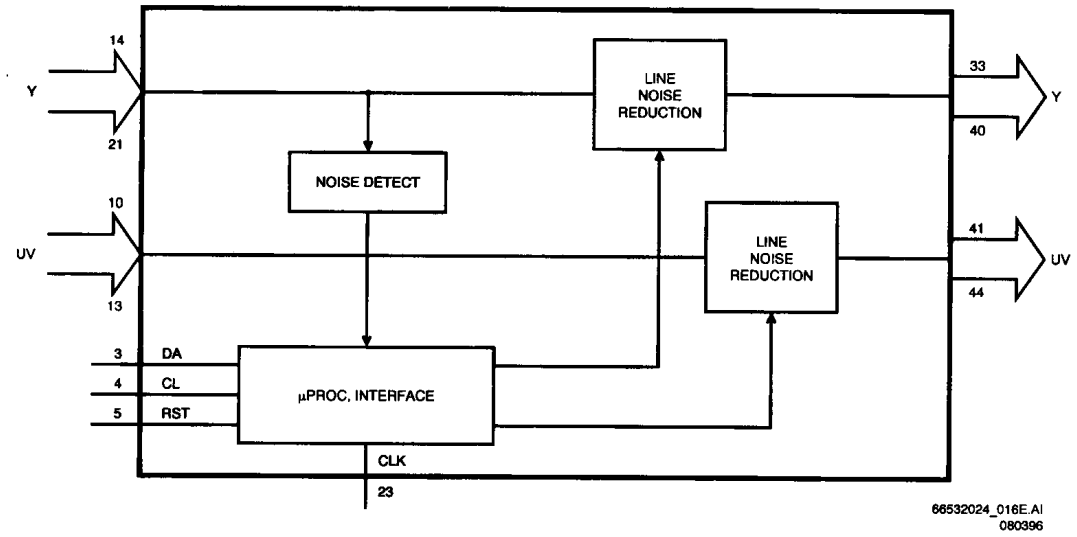


BENDIC SAA 4970 (IC 7450 in both feature boxes) M1 / M2

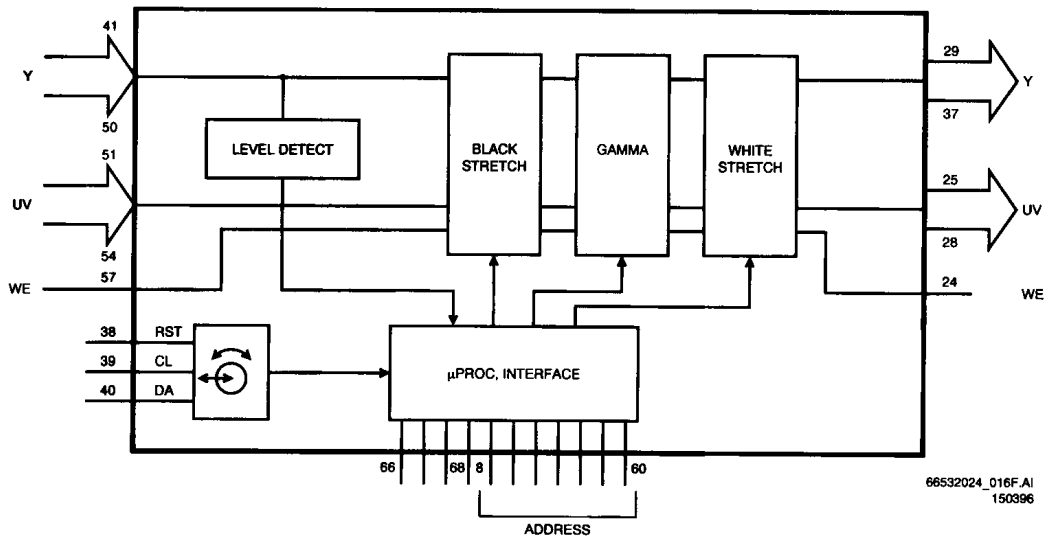


dans les boîtes de fonctions

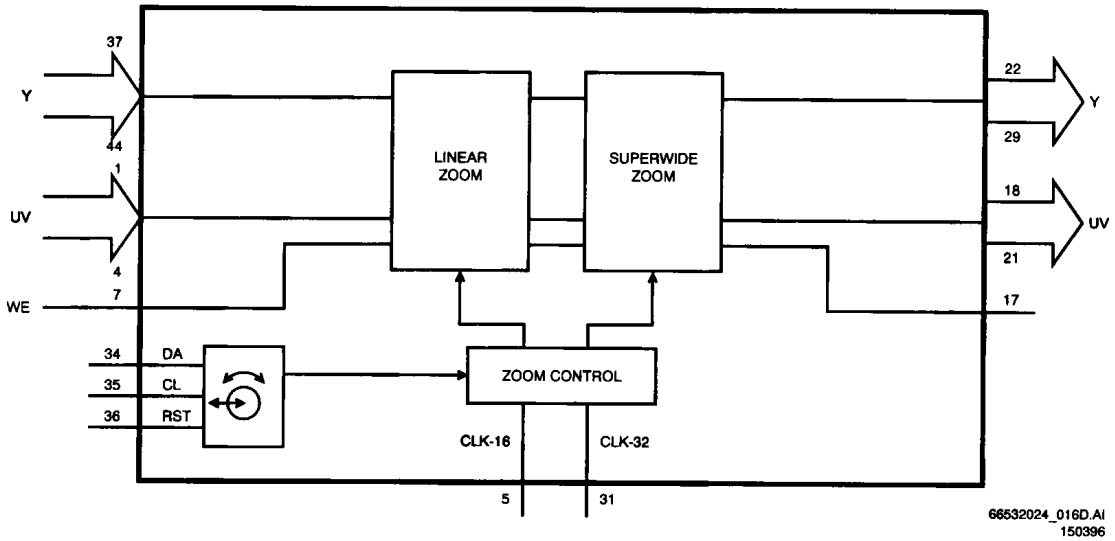
LIMERIC QFP44 (IC7005 on AI panel) N



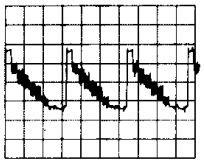
SMARTIC QFP80 (IC7008 on AI panel) N



PANIC PLC44 (IC7010 on AI panel) N

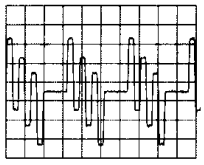


F1



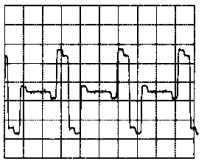
100mV/div
10µs/div

F2



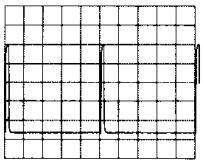
200mV/div
10µs/div

F3



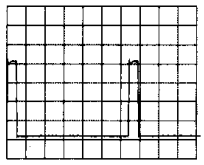
200mV/div
10µs/div

F4



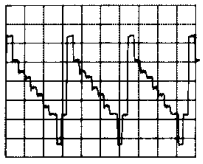
1V/div
2ms/div

F5



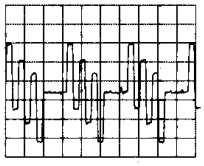
1V/div
5µs/div

F6



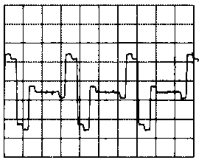
200mV/div
20µs/div

F7



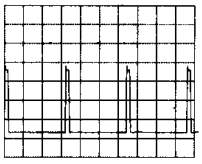
200mV/div
20µs/div

F8



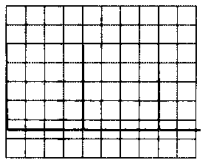
200mV/div
20µs/div

F9



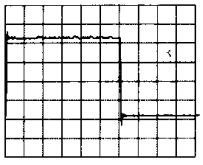
1V/div
20µs/div

F10



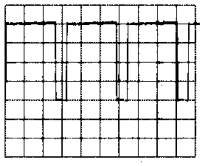
1V/div
5ms/div

F16



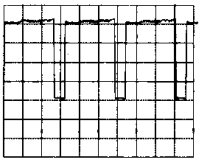
1V/div
0.5µs/div

F17



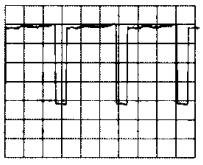
1V/div
20µs/div

F18



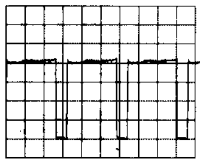
1V/div
10µs/div

F19



1V/div
10µs/div

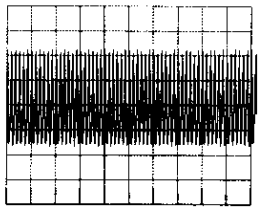
F20



1V/div
10µs/div

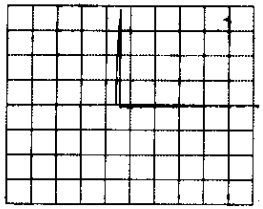
PCS 91 170

F11



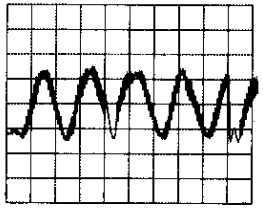
1V/div
0.5µs/div

F12



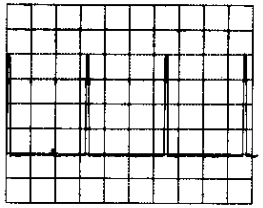
1V/div
50ms/div

F13



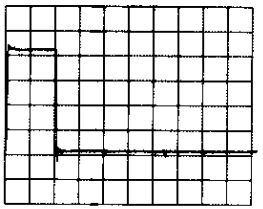
500V/div
50ns/div

F14



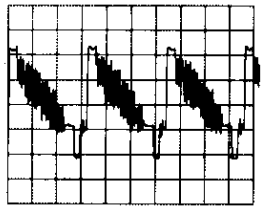
1V/div
20µs/div

F15



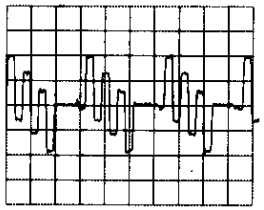
1V/div
0.5µs/div

F21



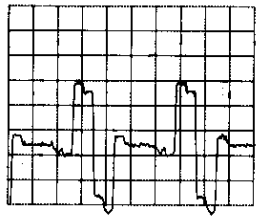
200mV/div
20µs/div

F22



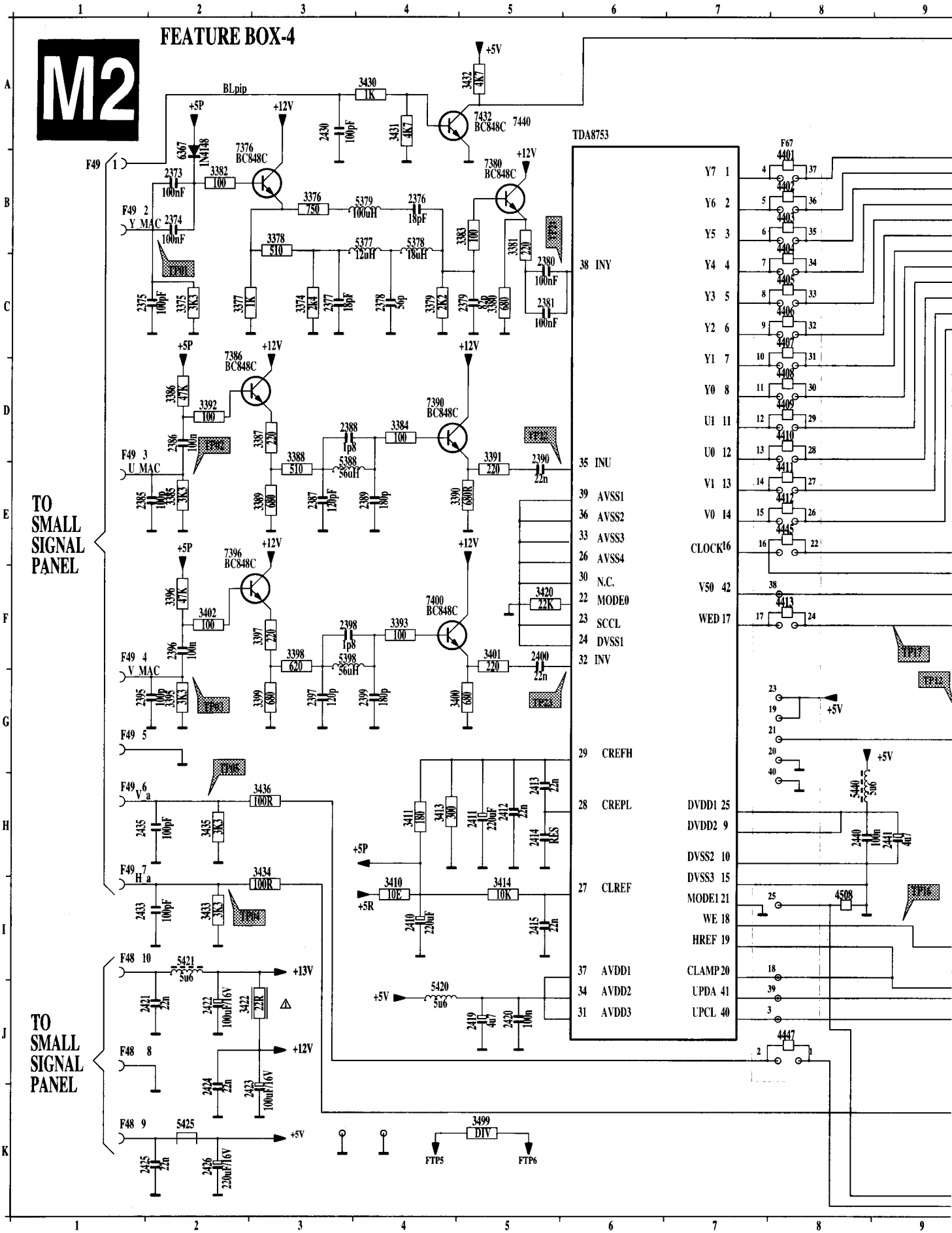
200mV/div
20µs/div

F23

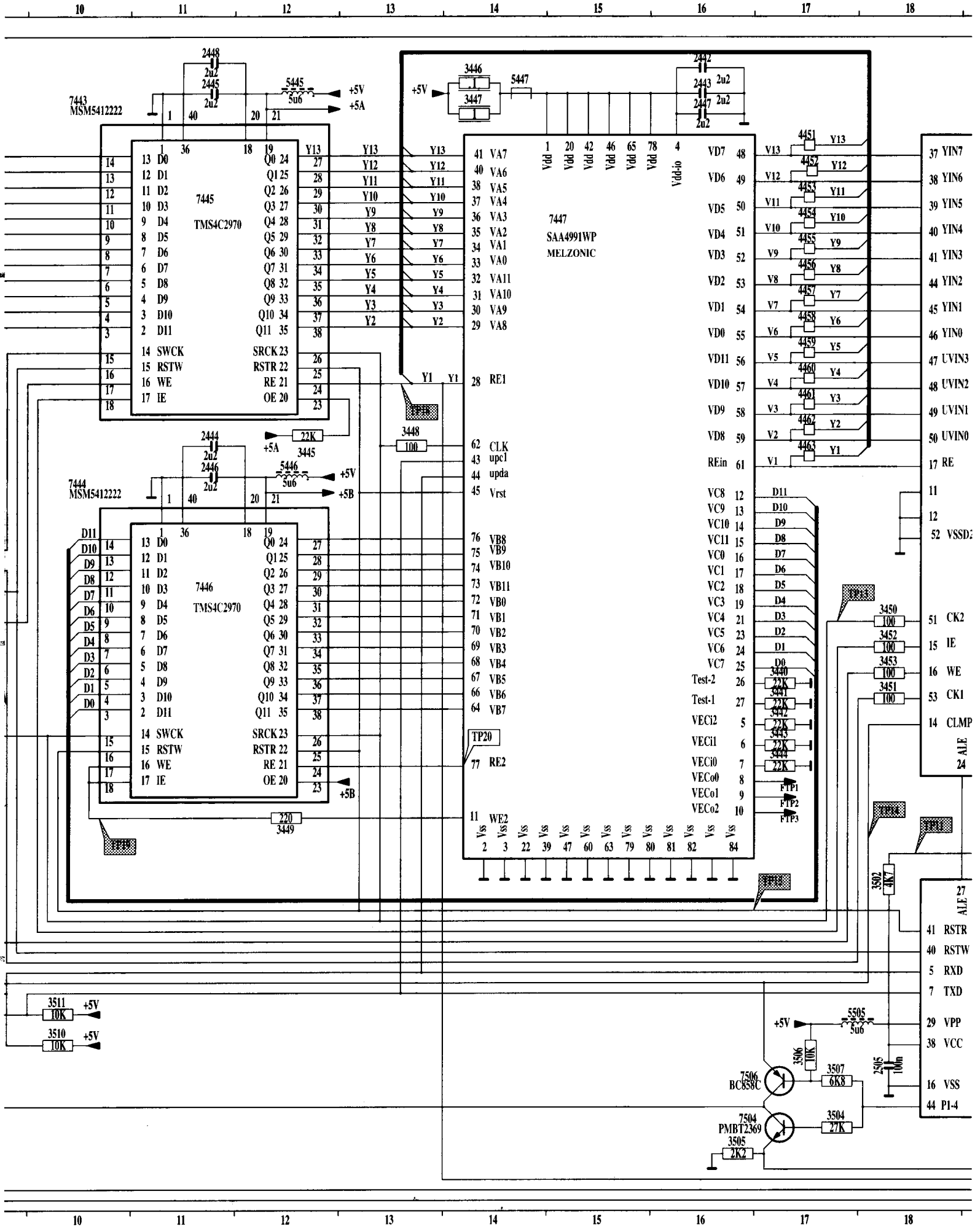


200mV/div
20µs/div

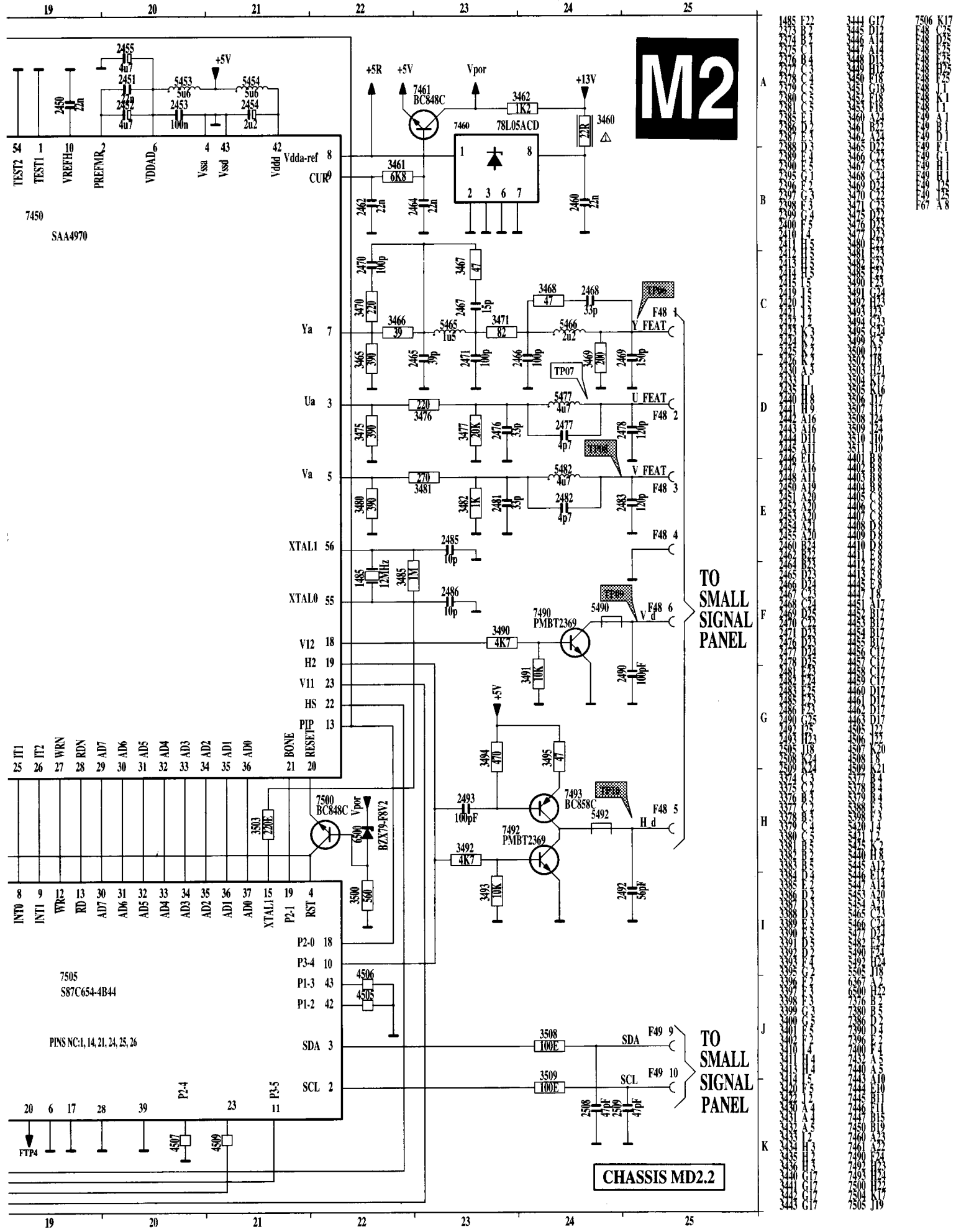
Feature Box (natural motion) panel /



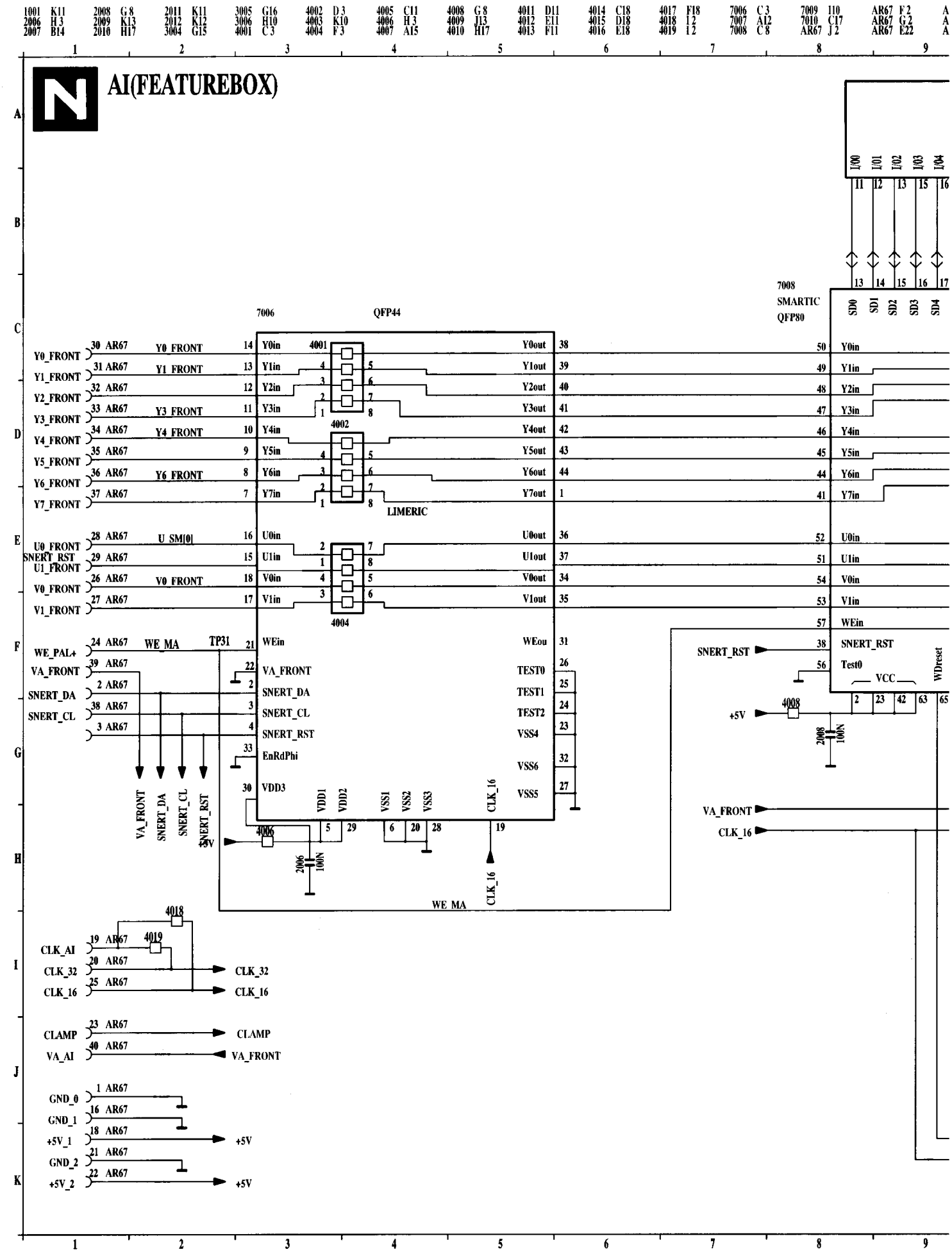
Feature-Box-Platine (Natürliche Bewegung) /



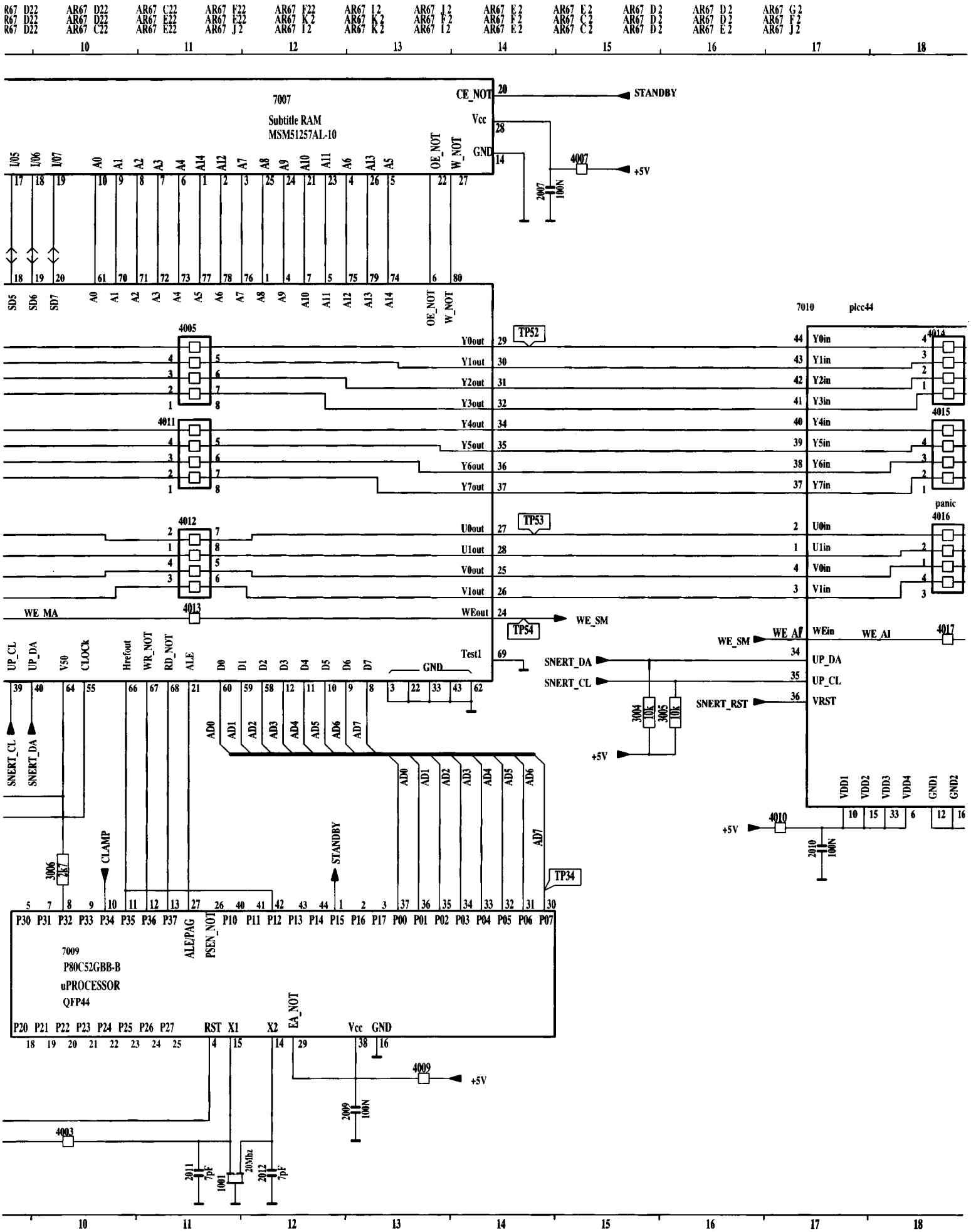
Platine Boîtier Numérique (mouvement natural)



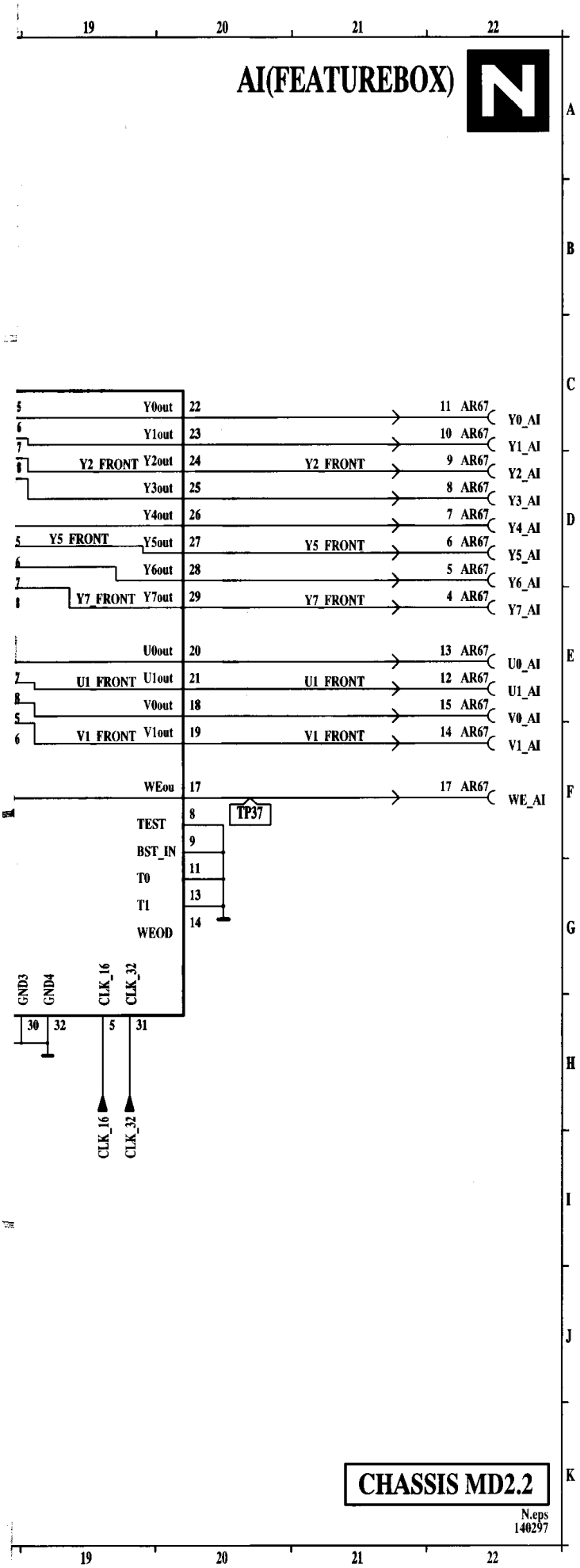
AI (Artificial Intelligence) panel /

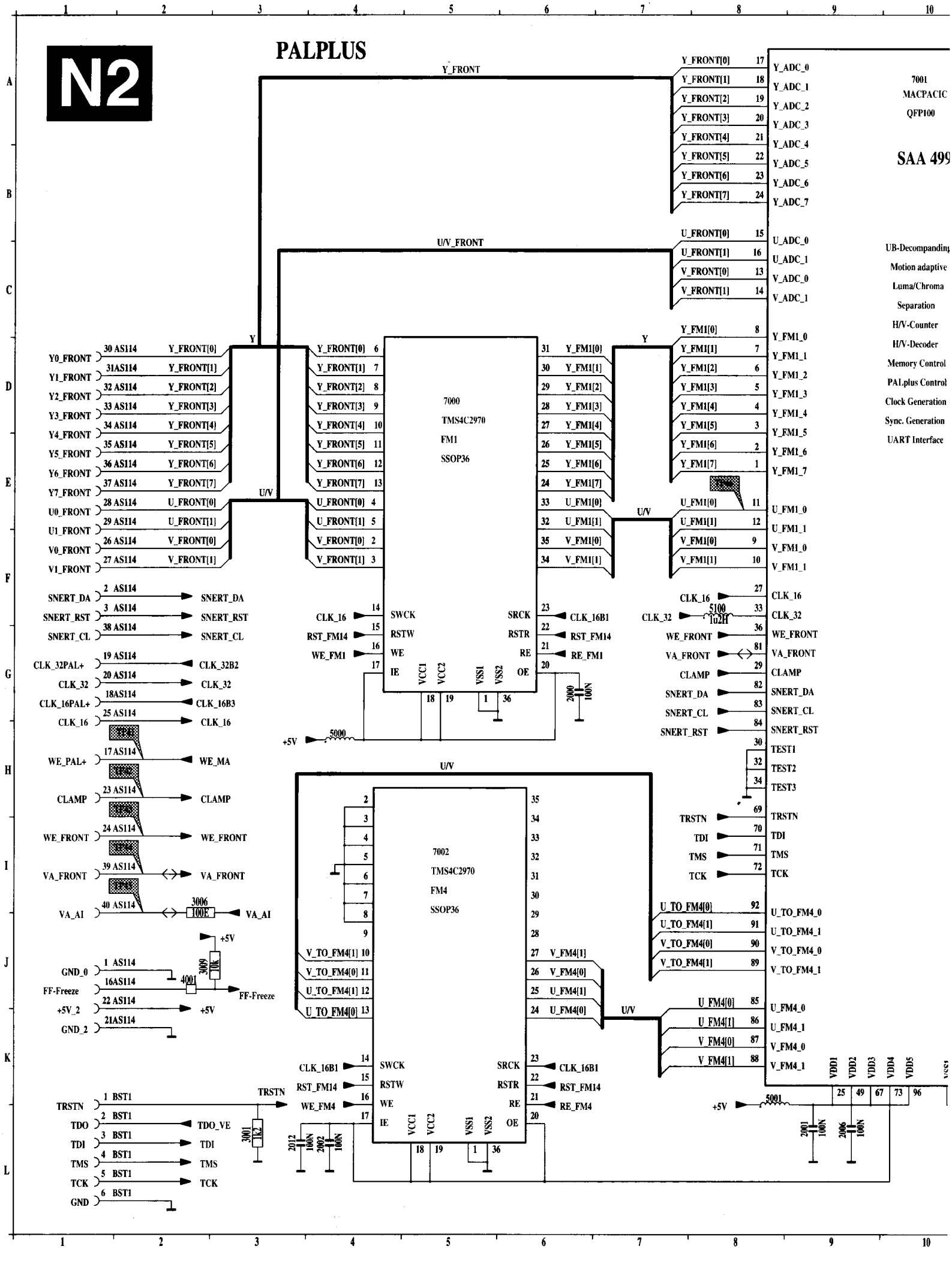


AI-(Künstliche Intelligenz)-Platine /

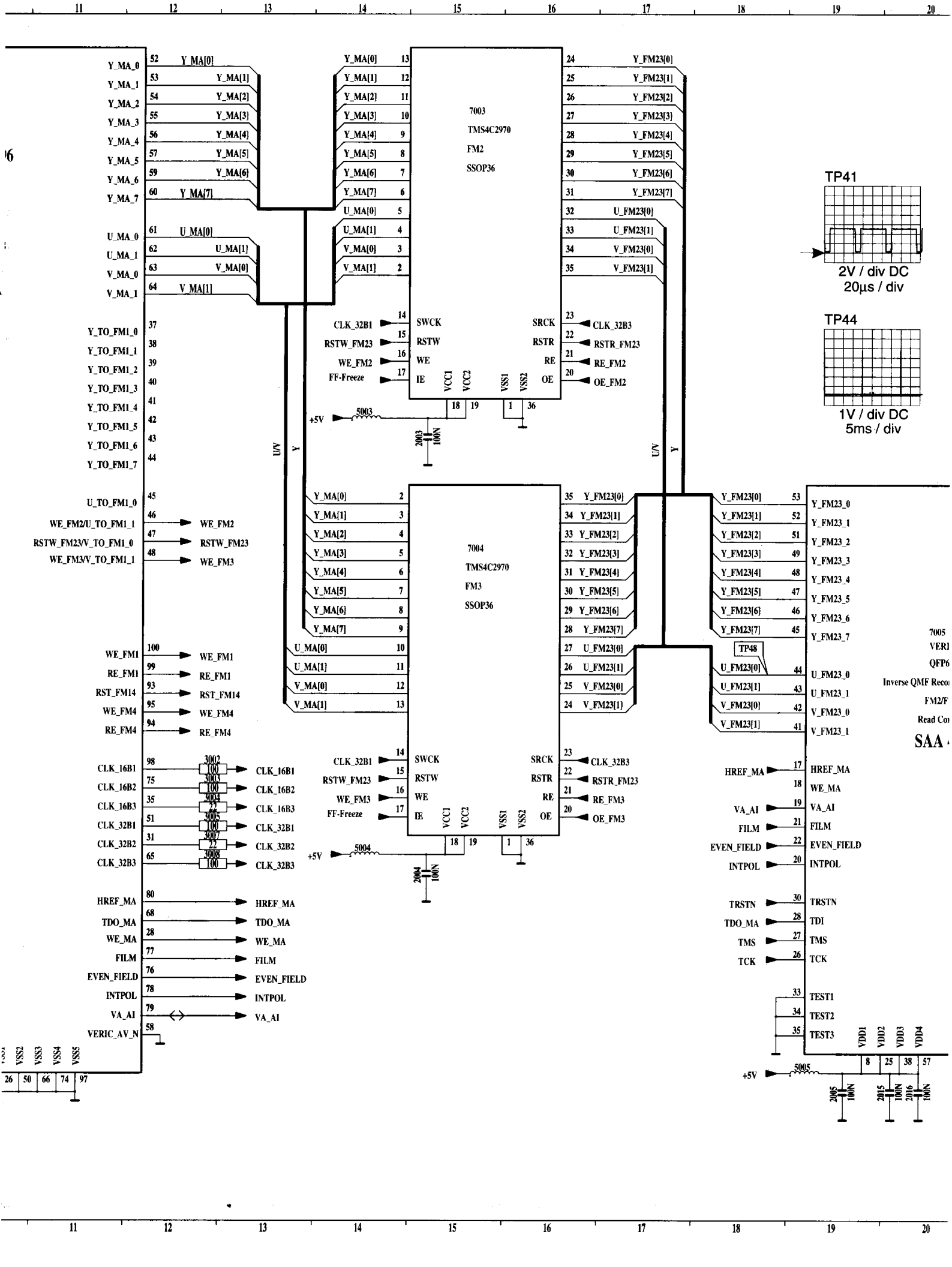


Platine AI (Intelligence Artificielle)

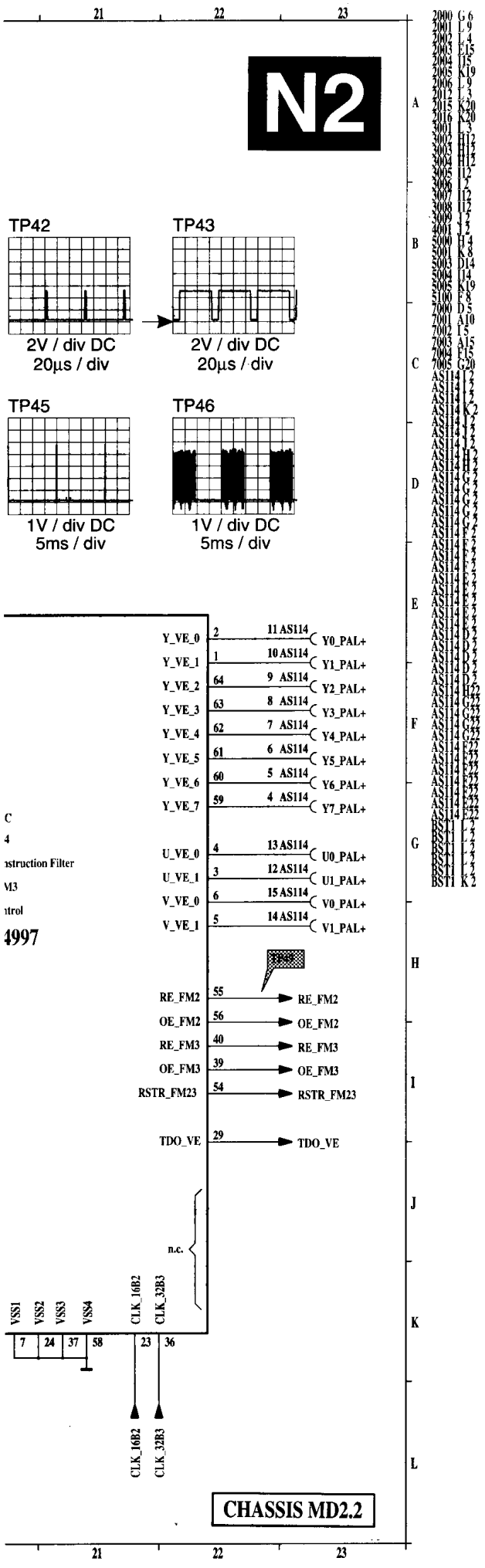



N2
PALPLUS
7001
MACPACIC
QFP100
SAA 499
UB-Decompanding
Motion adaptive
Luma/Chroma
Separation
H/V-Counter
H/V-Decoder
Memory Control
PALplus Control
Clock Generation
Sync. Generation
UART Interface
7000
TMS4C2970
FM1
SSOP36
7002
TMS4C2970
FM4
SSOP36
Y_FRONT
U/V_FRONT
Y
U/V
+5V
5000
5001
5100
1u2H
3006
100E
3009
10k
4001
3001
1k2
2000
100N
2001
100N
2006
100N
2012
100N
2002
100N
Y0_FRONT
Y1_FRONT
Y2_FRONT
Y3_FRONT
Y4_FRONT
Y5_FRONT
Y6_FRONT
Y7_FRONT
U0_FRONT
U1_FRONT
V0_FRONT
V1_FRONT
SNERT_DA
SNERT_RST
SNERT_CL
CLK_32PAL+
CLK_32
CLK_16PAL+
CLK_16
WE_PAL+
CLAMP
WE_FRONT
VA_FRONT
VA_AI
GND_0
FF-Freeze
+5V_2
GND_2
TRSTN
TDO
TDI
TMS
TCK
GND
TDO_VE
CLK_32B2
CLK_16B3
WE_MA
CLK_16B1
RST_FM14
RE_FM1
RE_FM4
WE_FM1
WE_FM4
TEST1
TEST2
TEST3
U_TO_FM4_0
U_TO_FM4_1
V_TO_FM4_0
V_TO_FM4_1
U_FM4_0
U_FM4_1
V_FM4_0
V_FM4_1
VDD1
VDD2
VDD3
VDD4
VDD5

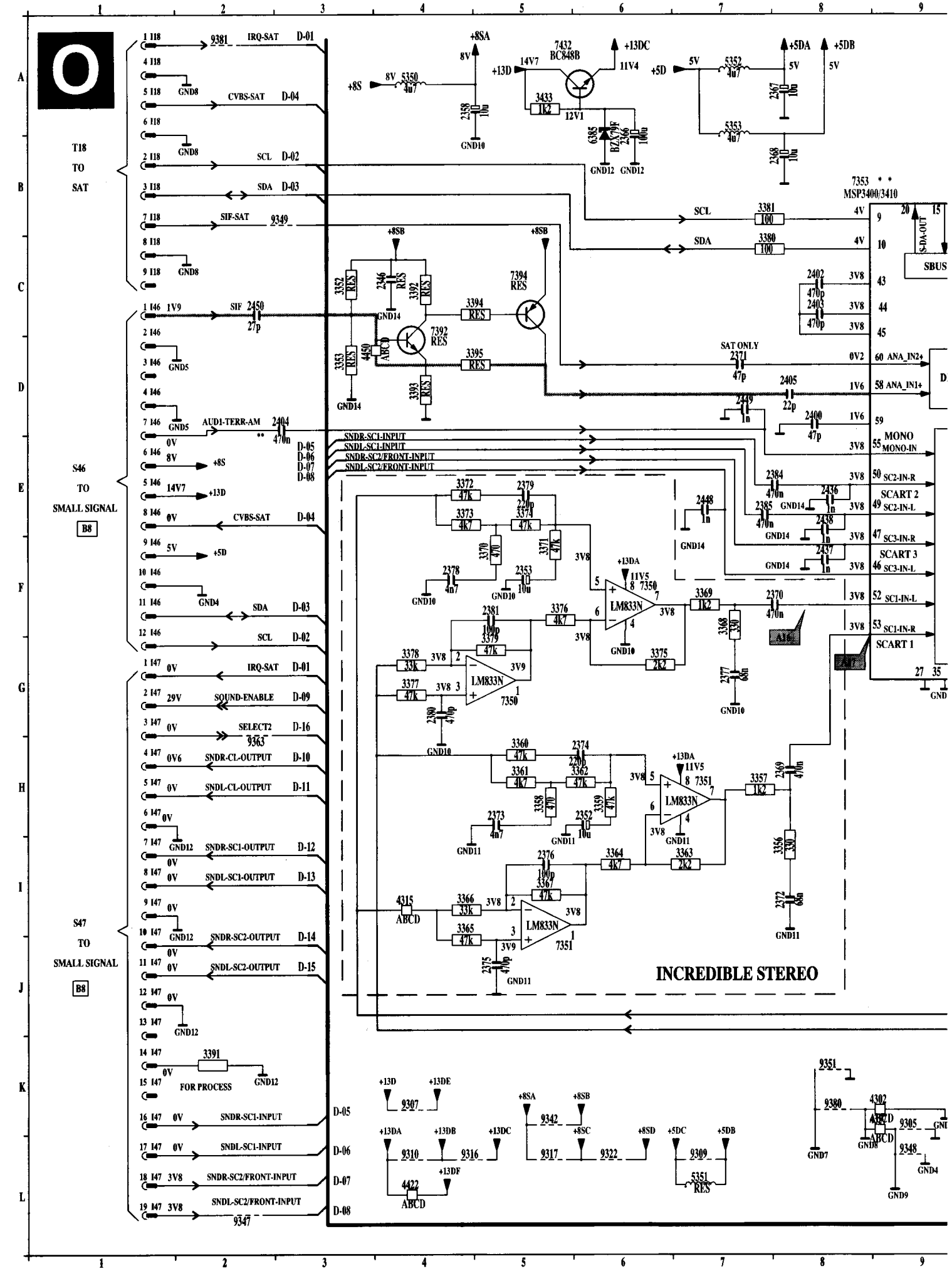
Platine PALplus

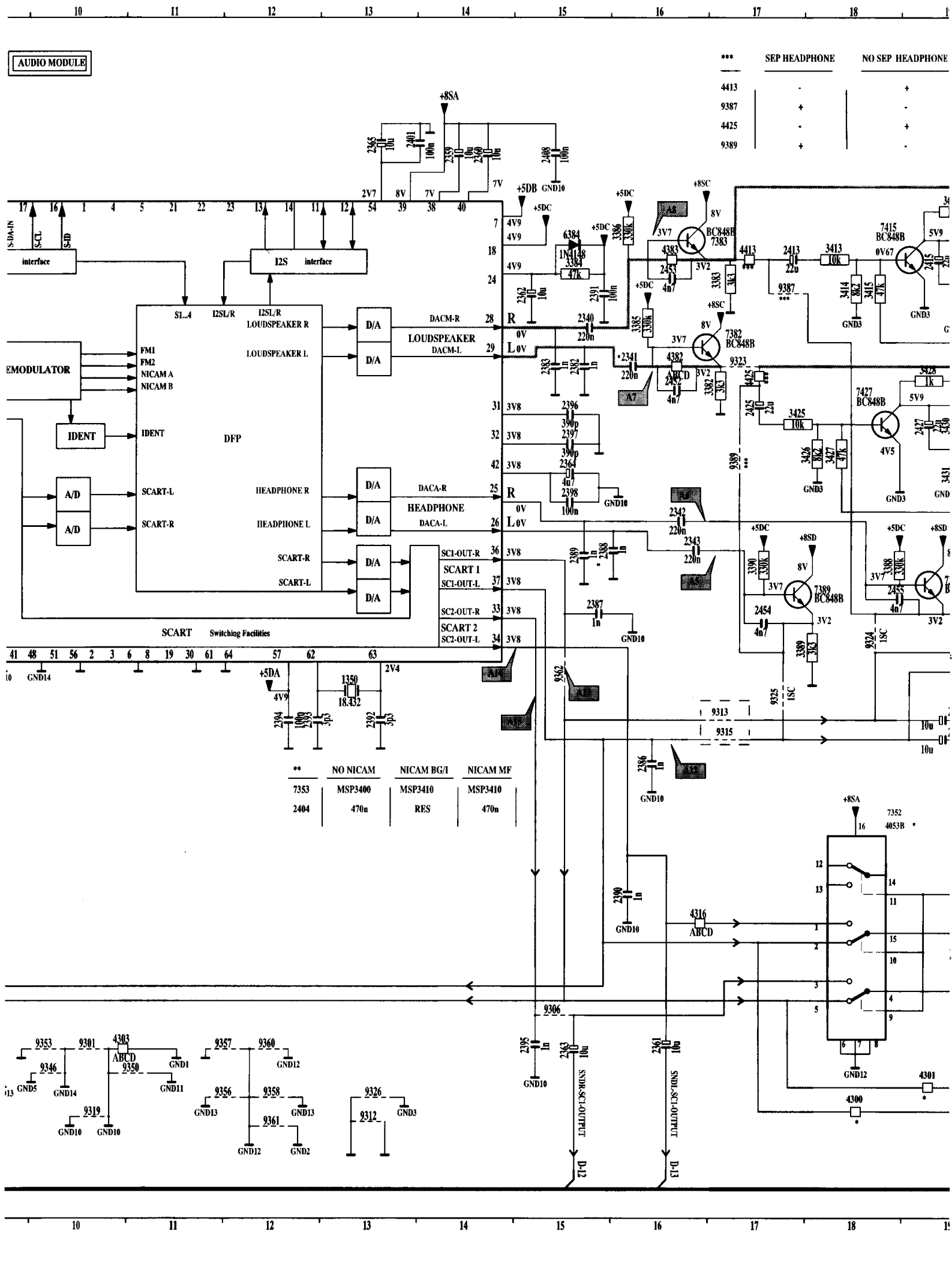


PALplus panel / PALplus-Pla

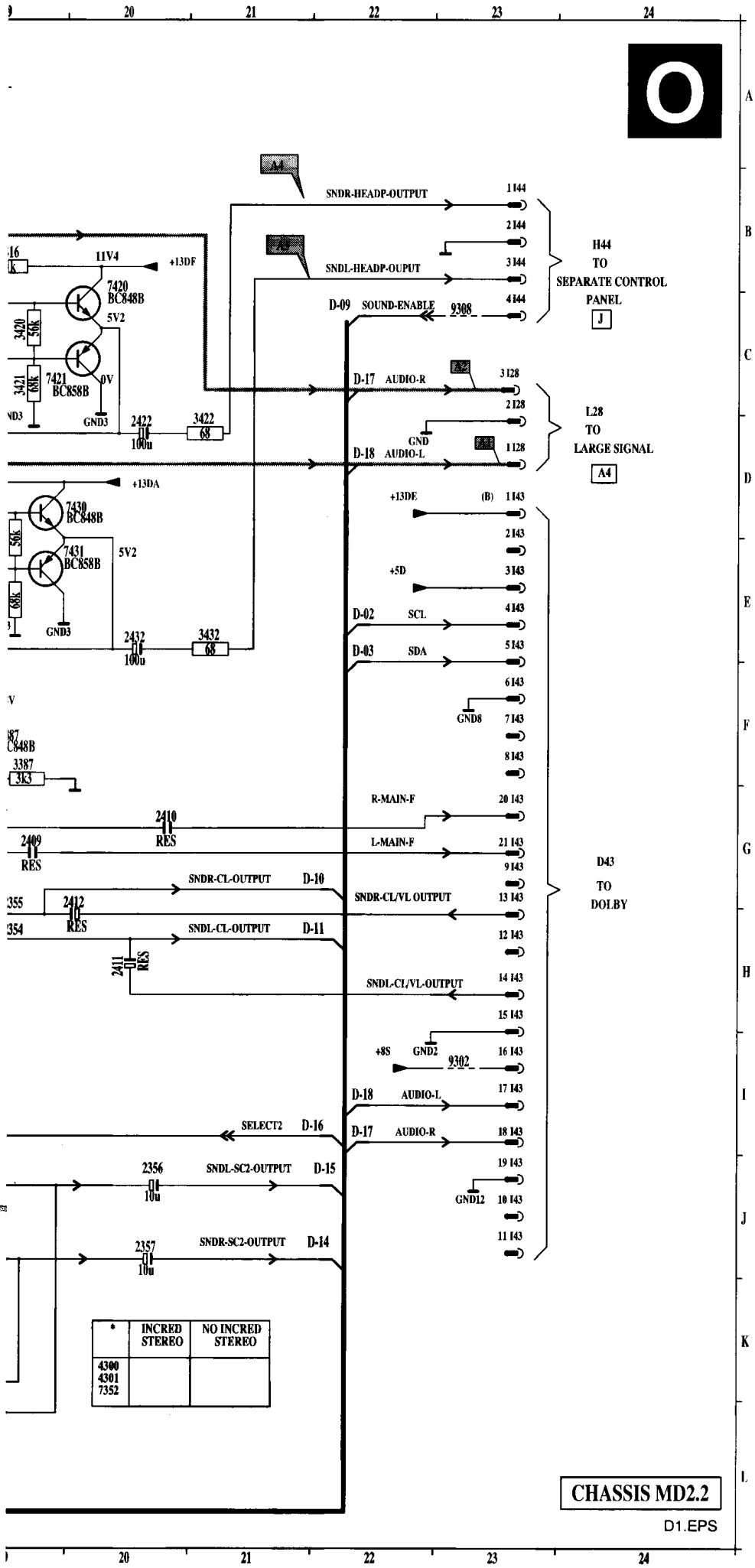


Audio module (no dolby) /




AUDIO MODULE
*** SEP HEADPHONE NO SEP HEADPHONE
4413 - +
9387 + -
4425 - +
9389 + -
+8SA
+5DB
+5DC
+8SC
+8SD
+5DA
GND10
GND14
GND3
GND5
GND1
GND11
GND12
GND13
GND2
interface
I2S interface
S1...4
I2SL/R
LOUDSPEAKER R
LOUDSPEAKER L
DFP
FM1
FM2
NICAM A
NICAM B
IDENT
SCART-L
SCART-R
HEADPHONE R
HEADPHONE L
DACM-R
DACM-L
DACA-R
DACA-L
LOUDSPEAKER
HEADPHONE
SCART 1
SCART 2
SC1-OUT-R
SC1-OUT-L
SC2-OUT-R
SC2-OUT-L
SCART Switching Facilities
D/A
A/D
** NO NICAM NICAM BG/I NICAM MF
7353 MSP3400 MSP3410 MSP3410
2404 470n RES 470n
4316 ABCD
4303 ABCD
SNDR-SCI-OUTPUT
SNDL-SCI-OUTPUT
D-12
D-13

Module audio (non Dolby)



*	INCRED STEREO	NO INCRED STEREO
4300 4301 7352		

A1 AUDIO-L - 3KHz (volume increased) — 50mV / div AC, 0.5ms / div

A8 pin 28 item 7353 (LOUDSPEAKER-R, 1KHZ, incr. volume) — 50mV / div AC, 0.2ms / div

A2 AUDIO-R - 1KHz (volume level increased) — 50mV / div AC, 0.5ms / div

A12 pin 37 item 7353 (SC1-OUT-L, 3KHz) - PAL/STEREO — 1V / div DC, 0.2ms / div

A3 SNDL-HEADPH-OUT (3KHz, HP incr.volume, Incr. Snd OFF) — 0V5 / div AC, 0.2ms / div

A13 pin 36 item 7353 (SC1-OUT-R, 1KHz) — 1V / div DC, 0.2ms / div

A4 SNDR-HEADPH-OUT (1KHz, HP incr. volume, Incr. Snd OFF) — 0V5 / div AC, 0.2ms / div

A14 pin 34 item 7353 (SC2-OUT-L, 3KHz) — 1V / div DC, 0.2ms / div

A5 pin 26 item 7353 (HP-L OUT - 3KHz) — 0V1 / div AC, 0.2ms / div

A15 pin 33 item 7353 (SC2-OUT-R, 1KHz) — 1V / div DC, 0.2ms / div

A6 pin 25 item 7353 (HP-R OUT - 1KHz) — 0V1 / div AC, 0.2ms / div

A16 pin 52 item 7353 (SC1-IN-L, 3KHz, Incr. Sound ON)

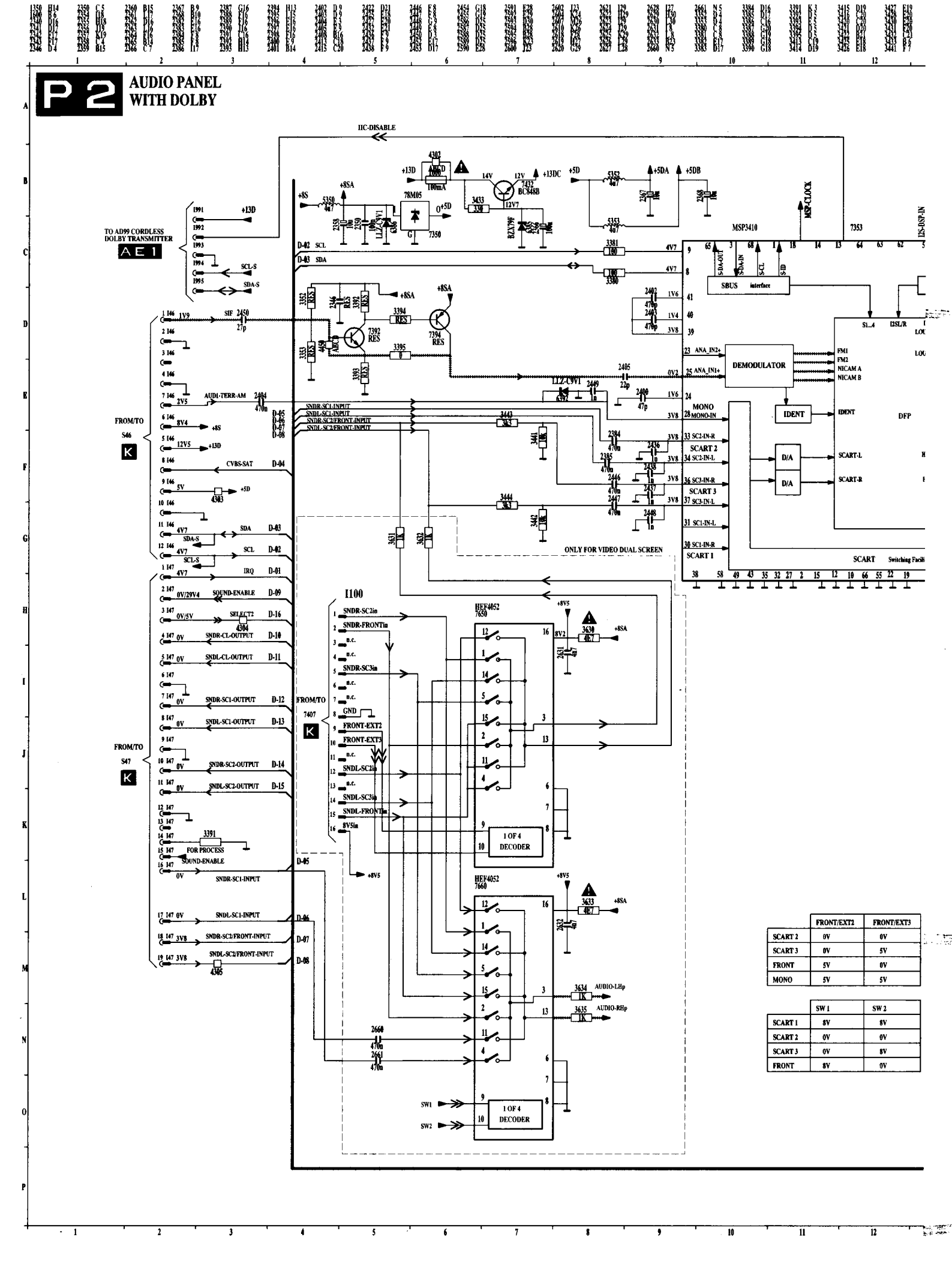
A17 pin 53 item 7353 (SC1-IN-R, 1KHz, Incr. Sound ON)

A7 pin 29 item 7353 (LOUDSPEAKER-L, 3 KHz, Incr. volume) — 50mV / div AC, 0.2ms / div

A17 / A16 — 0V2 / div AC, 0.2ms / div

= 0V

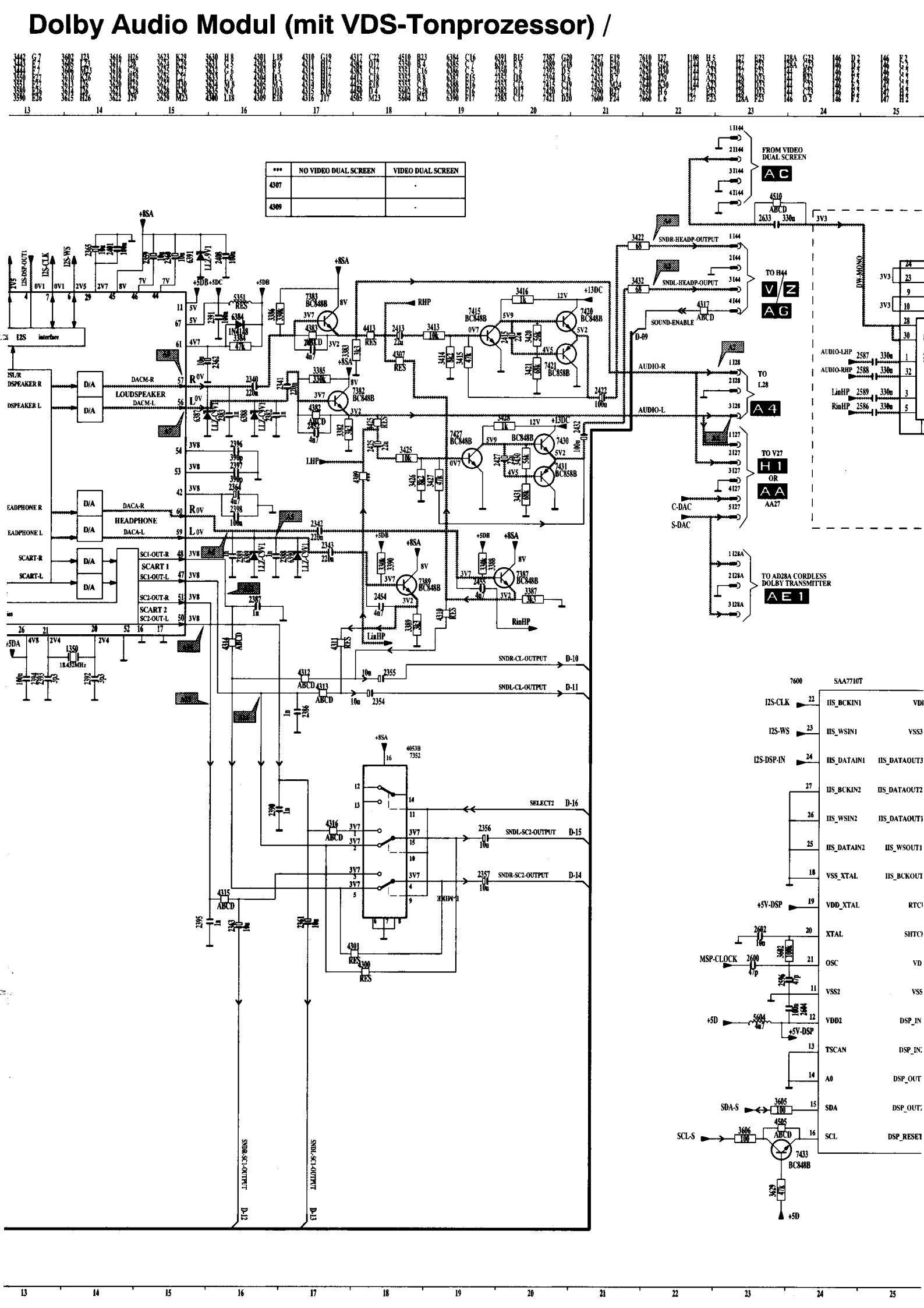
OSC_D1.CDR



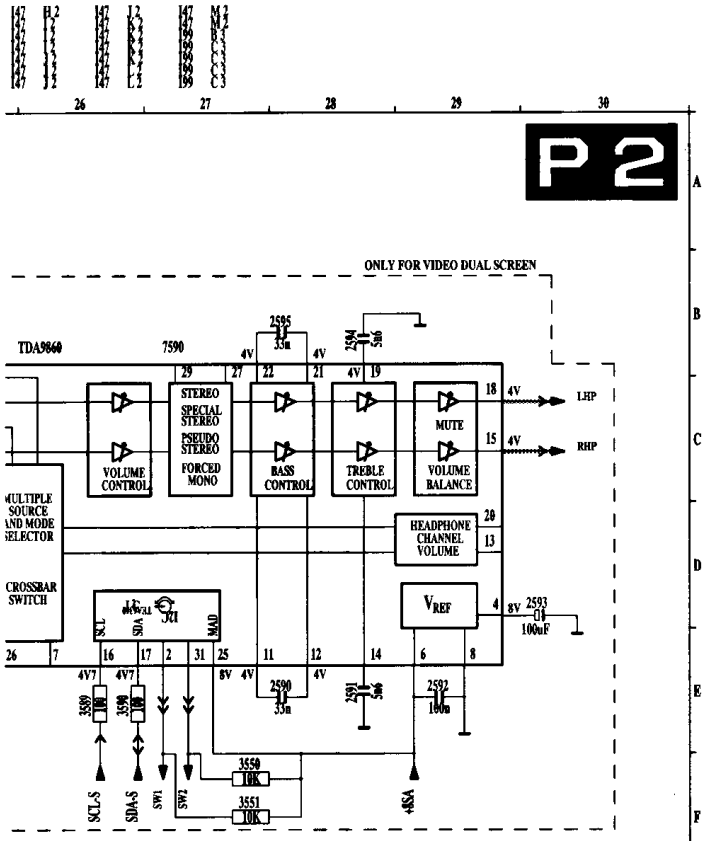
	FRONT/EXT2	FRONT/EXT3
SCART 2	0V	0V
SCART 3	0V	5V
FRONT	5V	0V
MONO	5V	5V

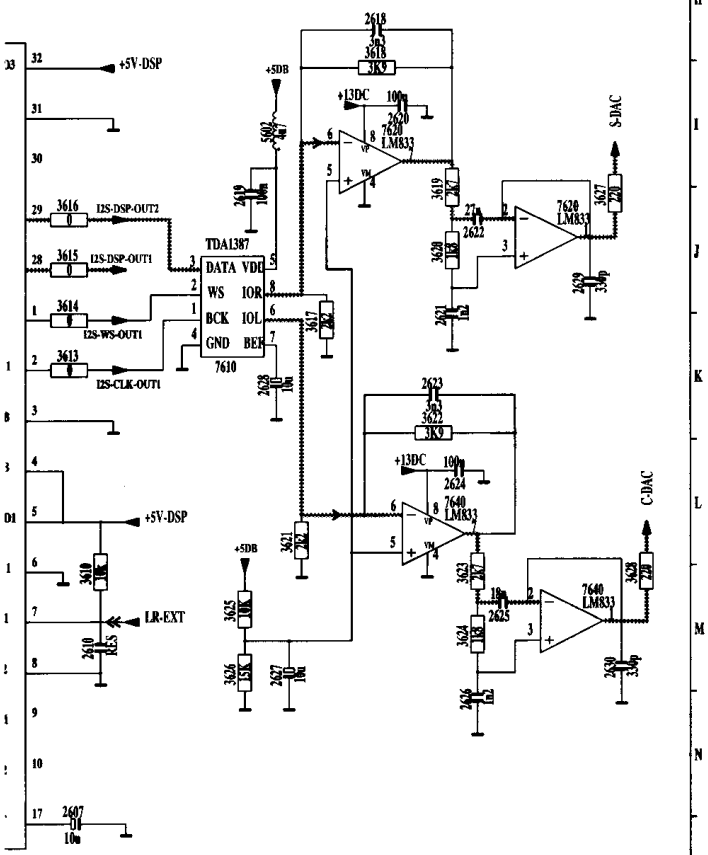
	SW 1	SW 2
SCART 1	8V	8V
SCART 2	0V	0V
SCART 3	0V	8V
FRONT	8V	0V

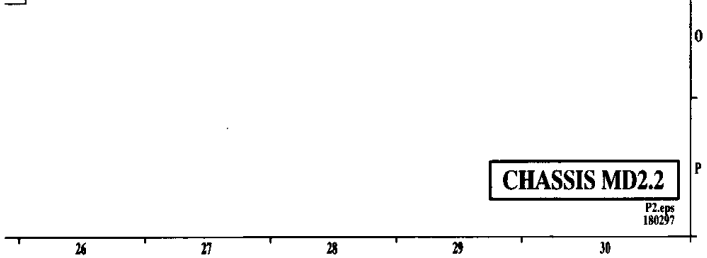
Dolby Audio Modul (mit VDS-Tonprozessor) /



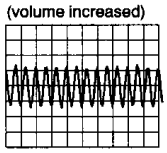
Module audio Dolby (avec traitement audio VDS)





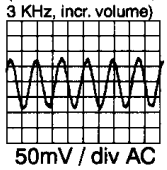


A1 AUDIO-L - 3KHz (volume increased)



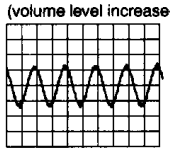
50mV / div AC
0.5ms / div

A7 pin 56 item 7353 (LOUDSPEAKER-L, 3 KHz, incr. volume)



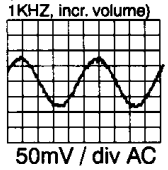
50mV / div AC
0.2ms / div

A2 AUDIO-R - 1KHz (volume level increased)



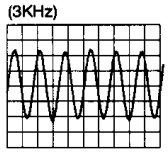
50mV / div AC
0.5ms / div

A8 pin 57 item 7353 (LOUDSPEAKER-R, 1KHZ, incr. volume)



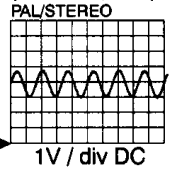
50mV / div AC
0.2ms / div

A3 SNDL-HEADPH-OUT (3KHz)



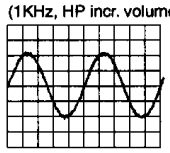
0V5 / div AC
0.2ms / div

A12 pin 48 item 7353 (SC1-OUT-L, 3KHz) - PAL/STEREO



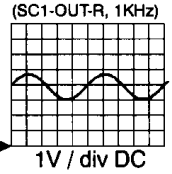
1V / div DC
0.2ms / div

A4 SNDR-HEADPH-OUT (1KHz, HP incr. volume)



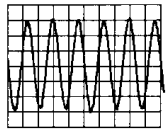
0V5 / div AC
0.2ms / div

A13 pin 47 item 7353 (SC1-OUT-R, 1KHz)



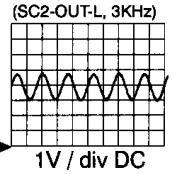
1V / div DC
0.2ms / div

A5 pin 59 item 7353 (HP-L OUT - 3KHz)



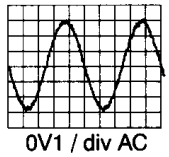
0V1 / div AC
0.2ms / div

A14 pin 50 item 7353 (SC2-OUT-L, 3KHz)



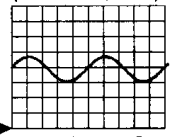
1V / div DC
0.2ms / div

A6 pin 60 item 7353 (HP-R OUT - 1KHz)



0V1 / div AC
0.2ms / div

A15 pin 51 item 7353 (SC2-OUT-R, 1KHz)

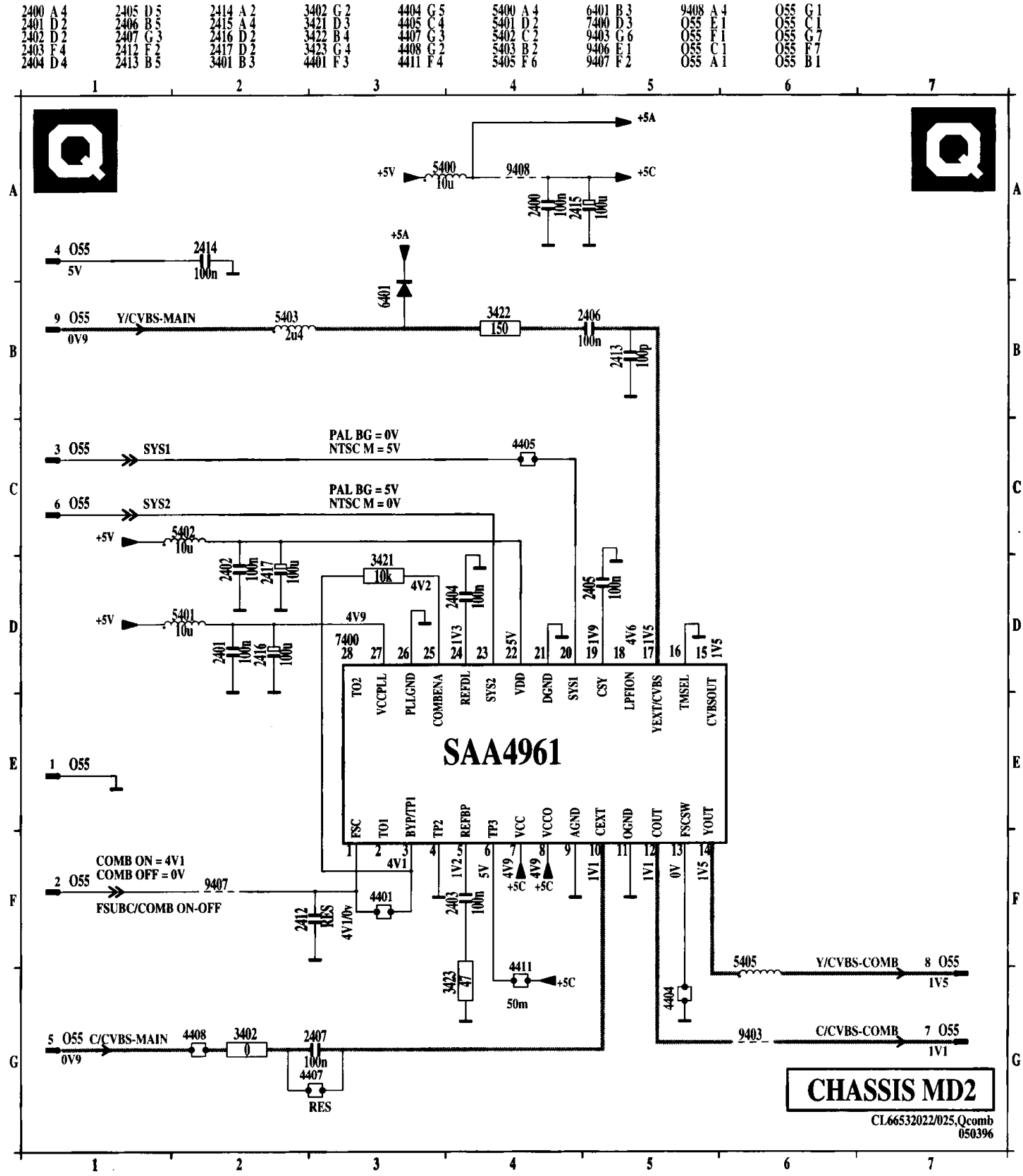


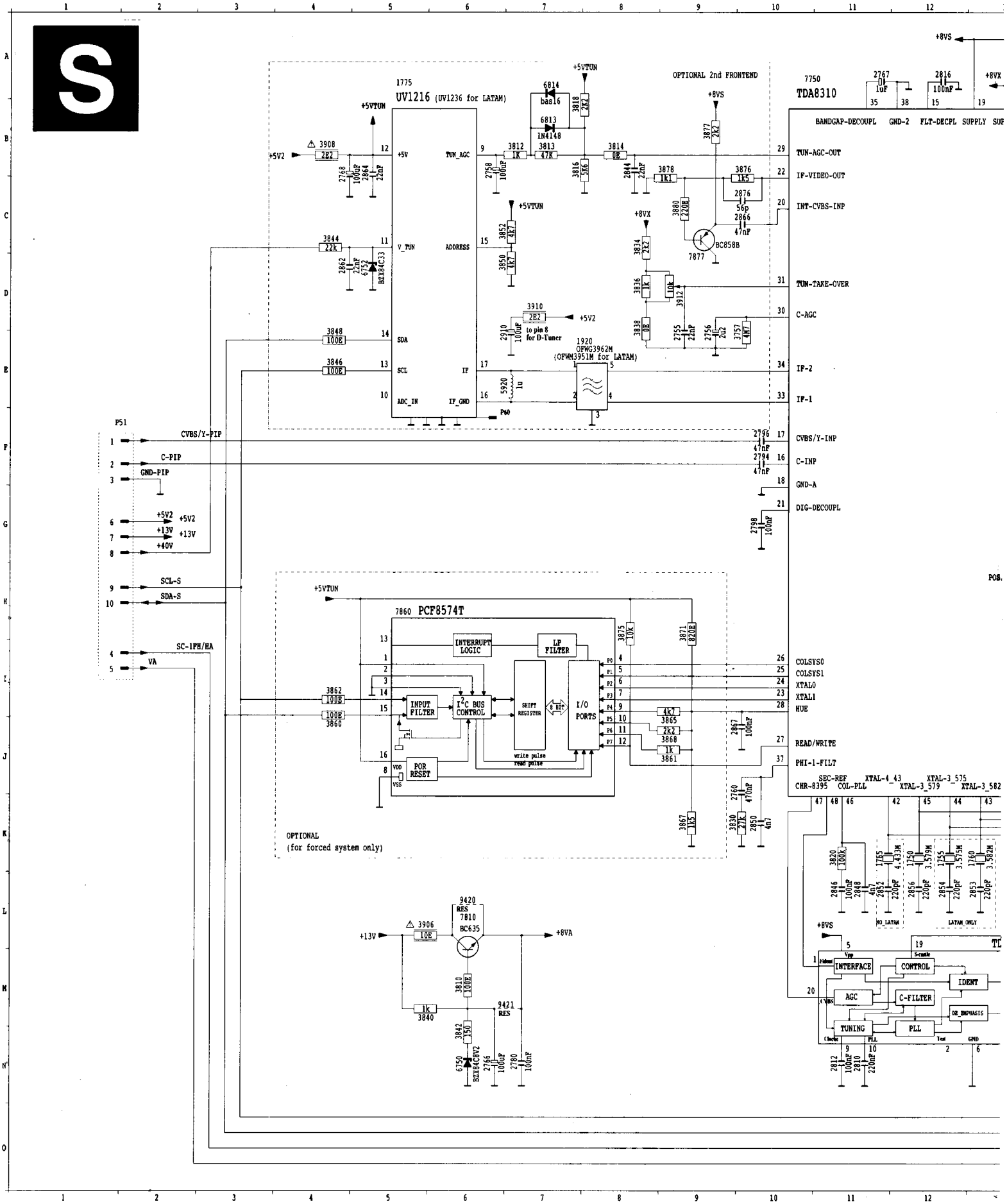
1V / div DC
0.2ms / div

→ = 0V

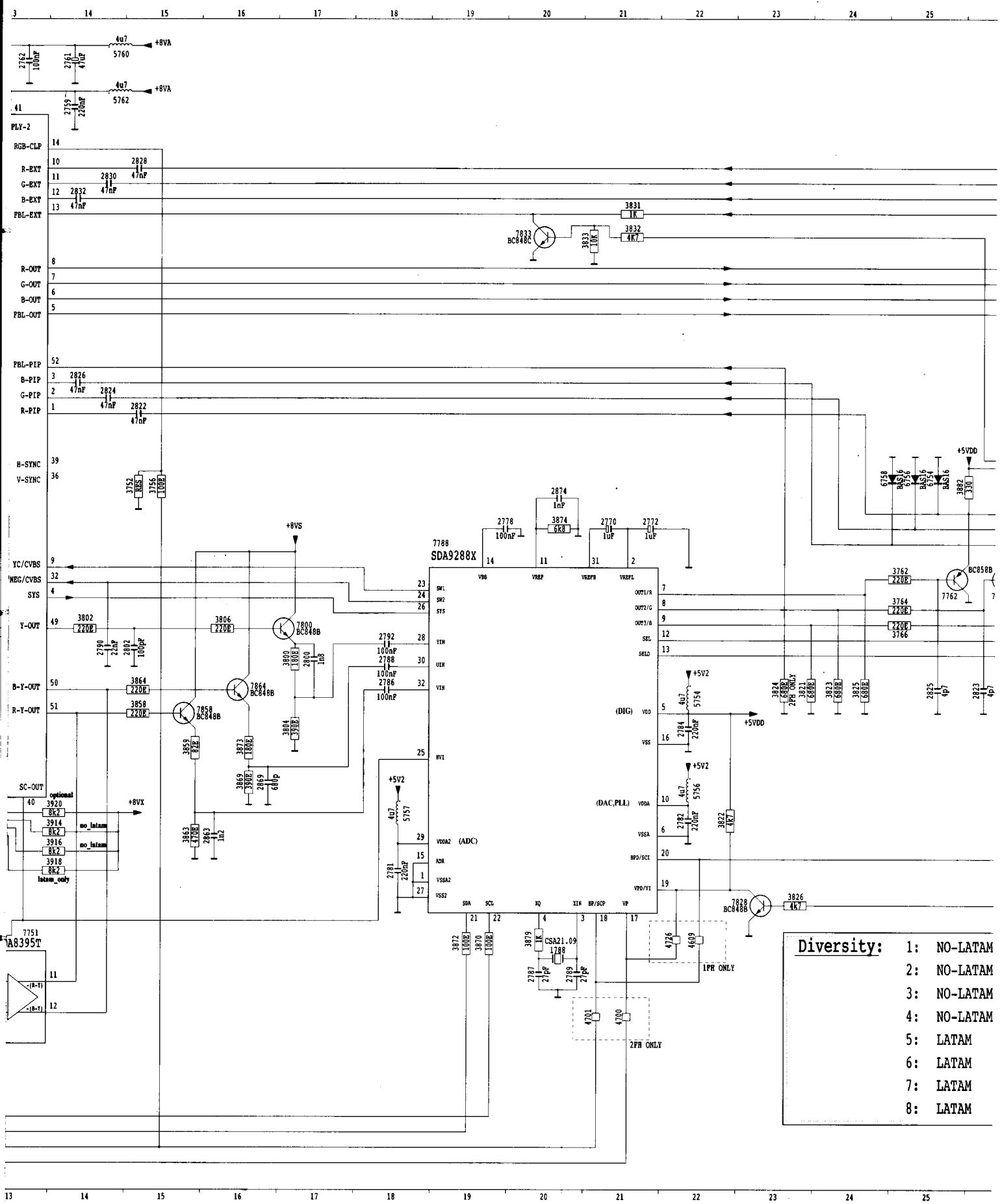
OSC_P2.CDR
260297

COMB filter module / Kammfilter-Modul / Module filtre en peigne




S
1775
UV1216 (UV1236 for LATAM)
OPTIONAL 2nd FRONTEND
7750
TDA8310
BANDGAP-DECOUPL
GND-2
FLT-DECPL
SUPPLY
TUN-AGC-OUT
IF-VIDEO-OUT
INT-CVBS-INP
TUN-TAKE-OVER
C-AGC
IF-2
IF-1
CVBS/Y-INP
C-INP
GND-A
DIG-DECOUPL
P51
CVBS/Y-PIP
C-PIP
GND-PIP
+5V2
+13V
+40V
SCL-S
SDA-S
SC-1FH/HA
VA
7860 PCF8574T
INTERRUPT LOGIC
LP FILTER
INPUT FILTER
I2C BUS CONTROL
SHIFT REGISTER
I/O PORTS
POR RESET
COLSYS0
COLSYS1
XTAL0
XTAL1
HUE
READ/WRITE
PHI-1-FILT
OPTIONAL
(for forced system only)
BC858B
BC635
+8VA
INTERFACE
CONTROL
IDENT
AGC
C-FILTER
TUNING
PLL

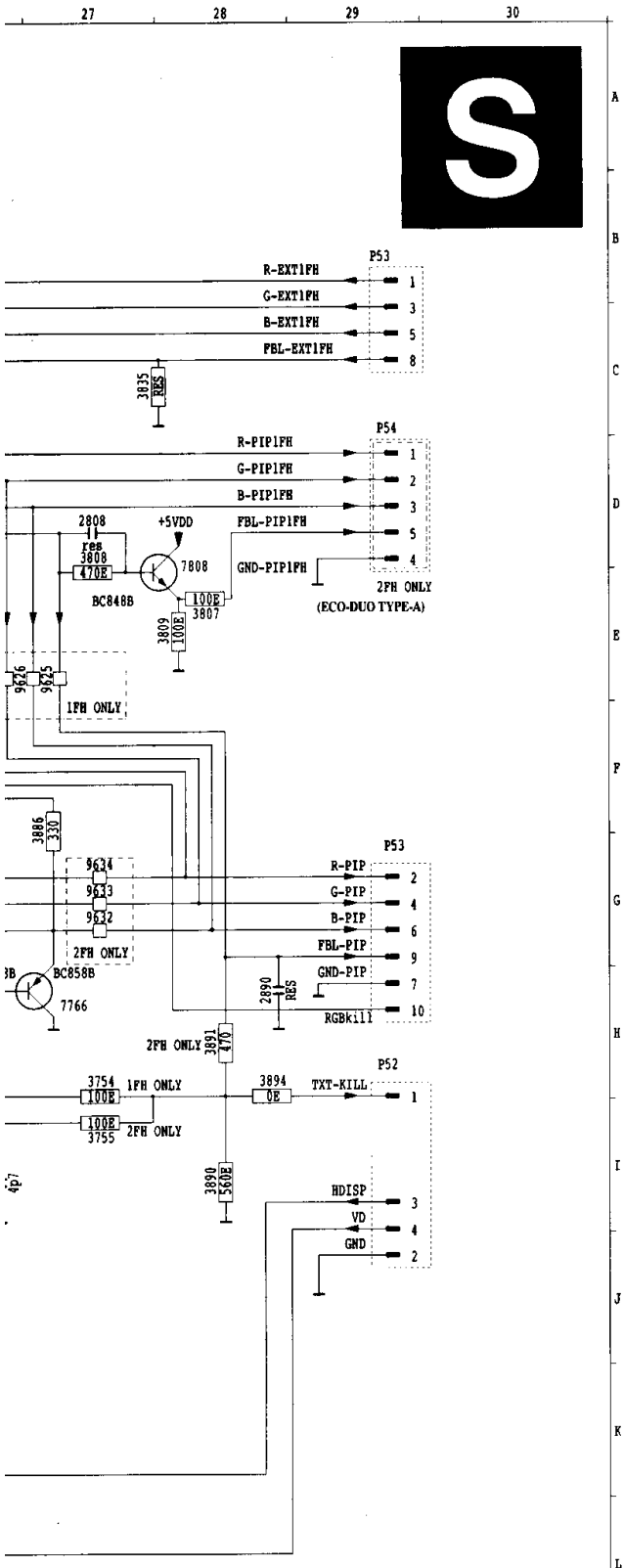
PIP2-Modul



Diversity:

1: NO-LATAM
2: NO-LATAM
3: NO-LATAM
4: NO-LATAM
5: LATAM
6: LATAM
7: LATAM
8: LATAM

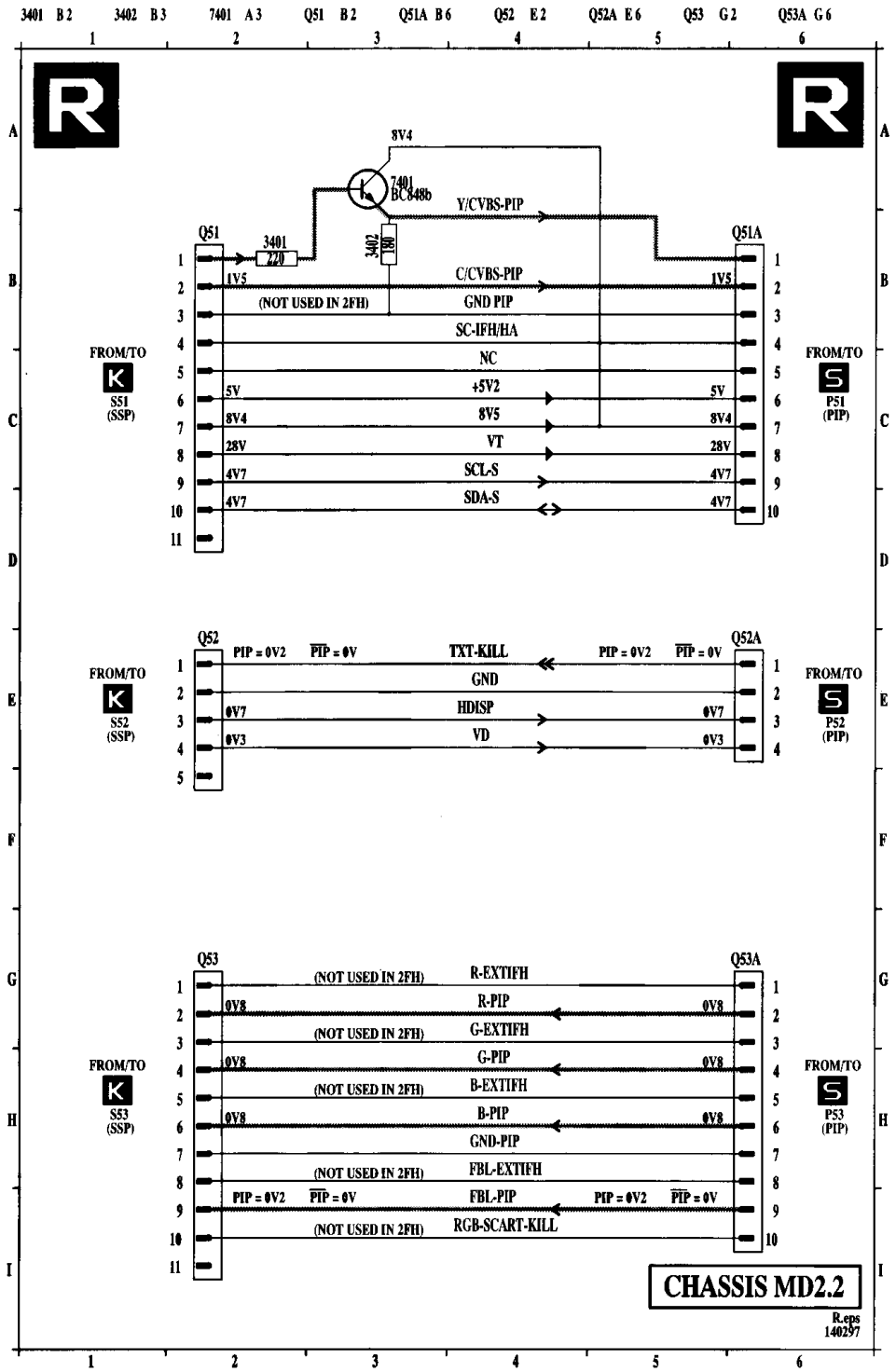
Module PIP2

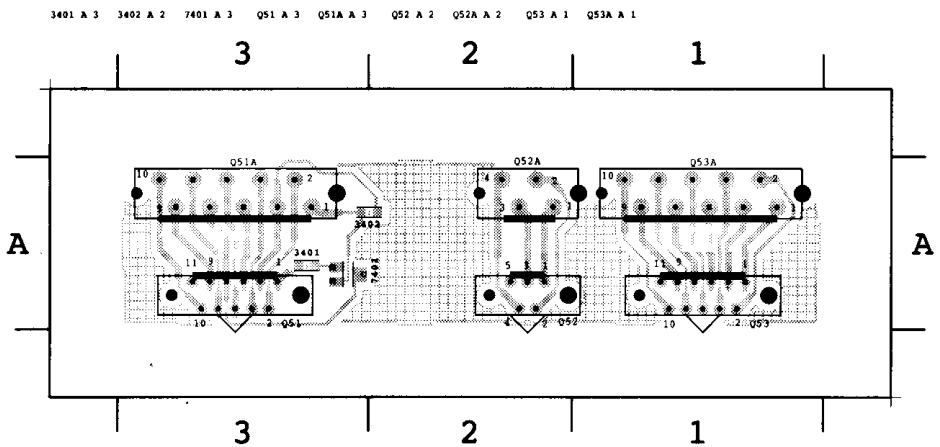


-FRONTEND / 1FH	
-FRONTEND / 2FH	
FRONTEND / 1FH	
FRONTEND / 2FH	
-FRONTEND / 1FH	
-FRONTEND / 2FH	
FRONTEND / 1FH	
FRONTEND / 2FH	

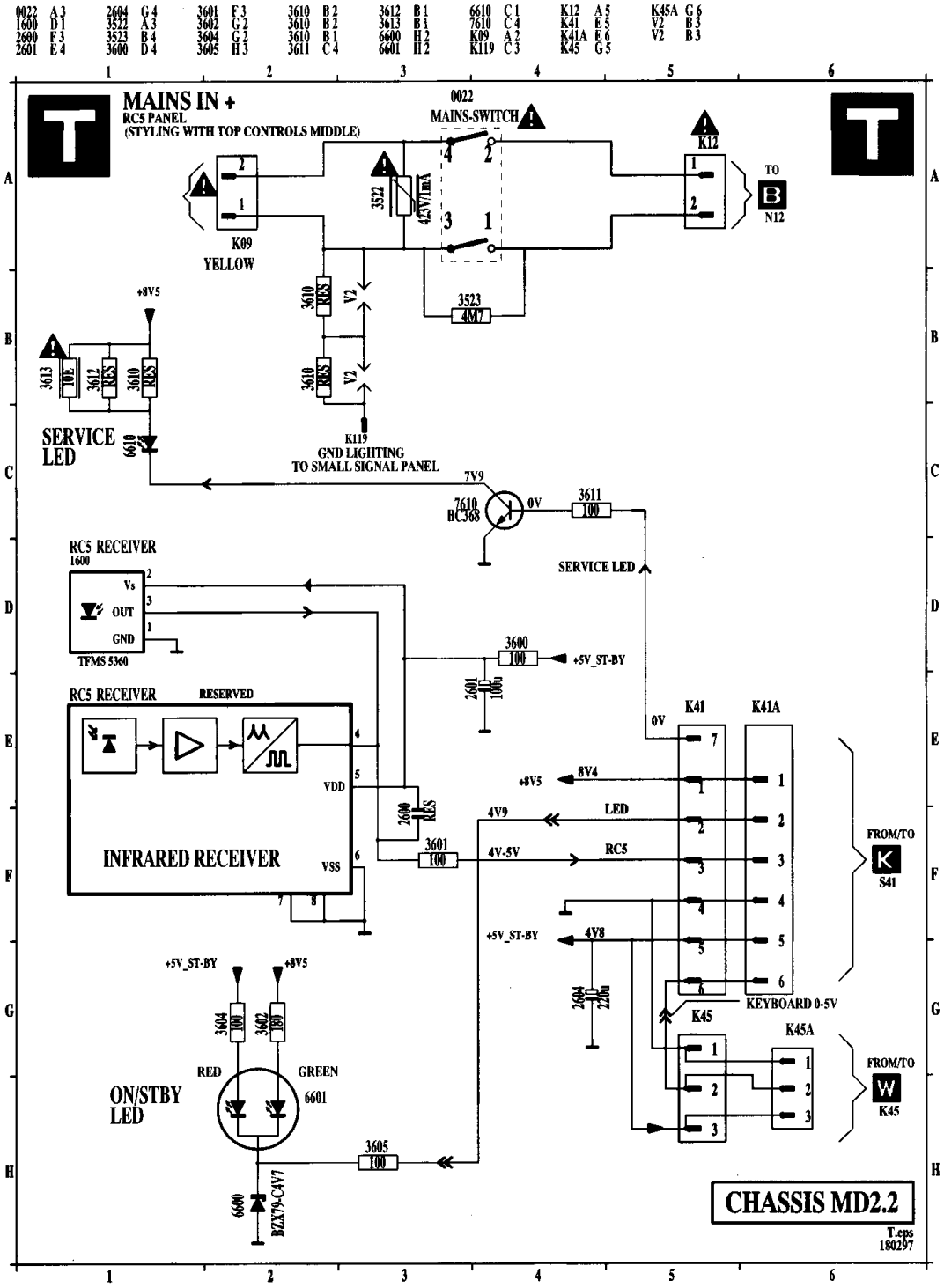
CHASSIS MD2.2

PIP interface panel / PIP-Schnittstellenplatine / Platine interface PIP (image incrustée)

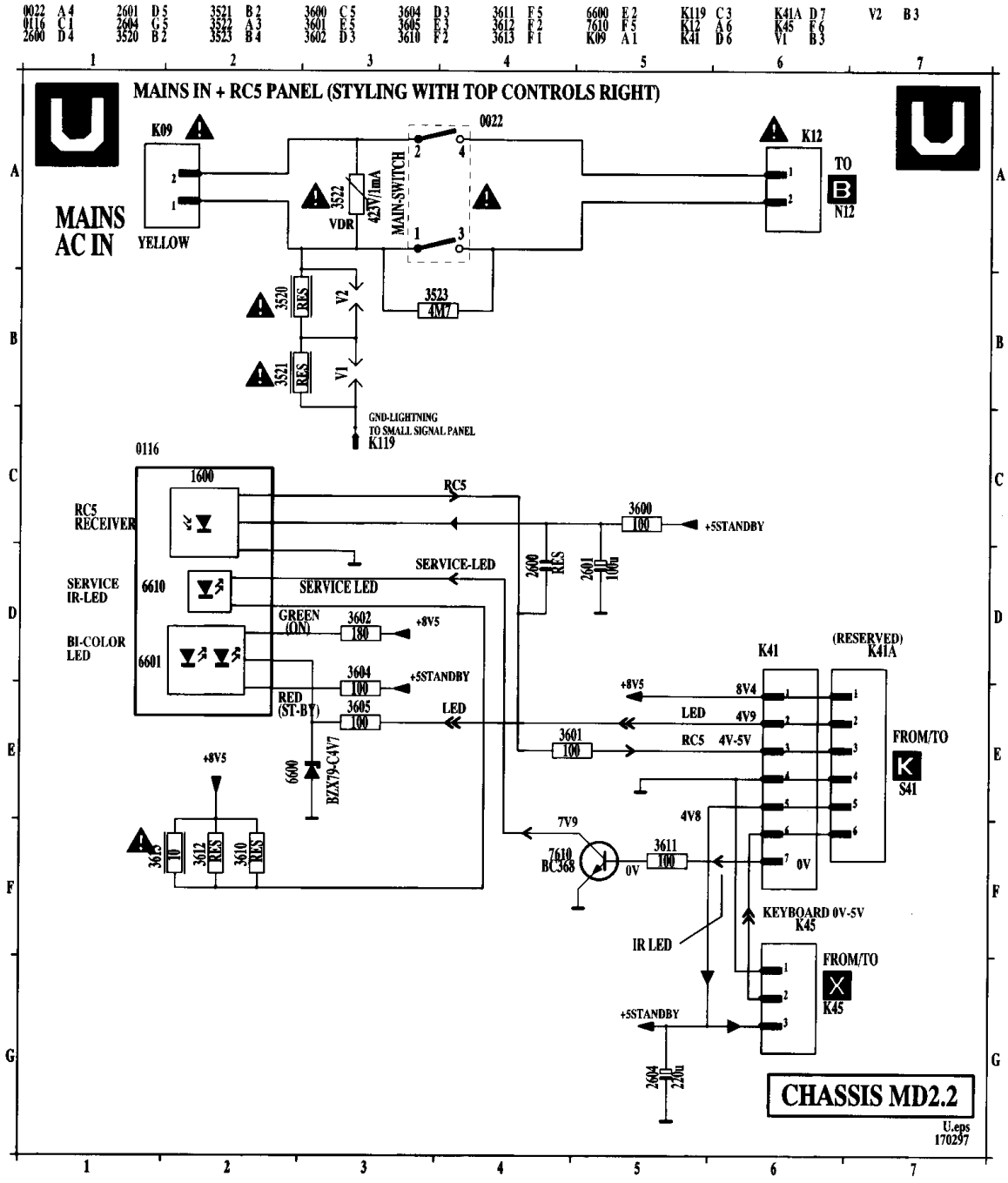




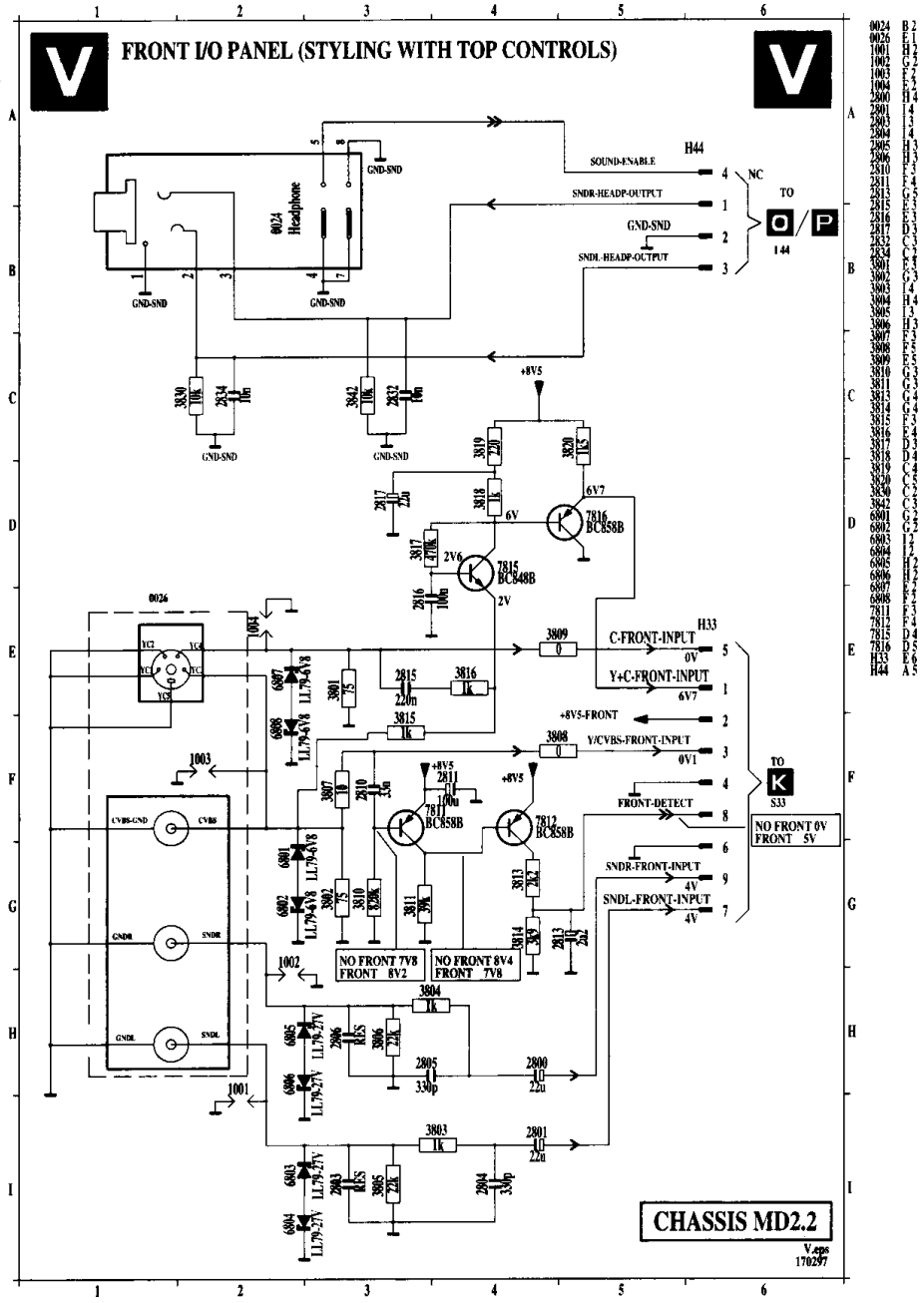
Mains input & RC5 panel (top control middle styling) / Netzeingang- & RC5-Platine (Bedienung mitte oben) / Platine entrée secteur & RC5 (style commande sur le haut, millieu)



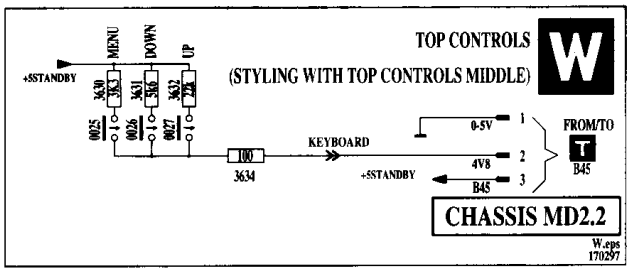
Mains input & RC5 panel (top control right styling) / Netzeingang- & RC5-Platine (Bedienung rechts oben) / Platine entrée secteur & RC5 (style commande sur le haut, droite)

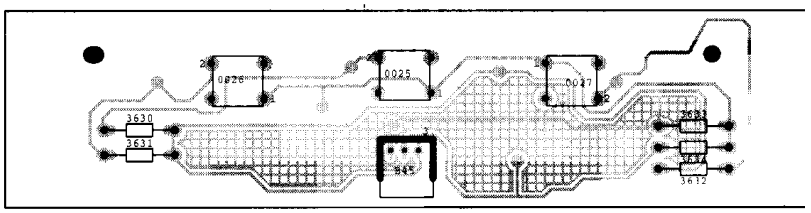


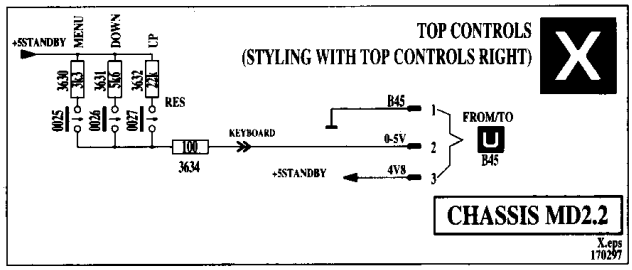
Front input/output panel (top control styling) / Front-Ein-/Ausgangsplatine (Bedienung oben) / Platine frontale entrée/sortie (style commande sur le haut)

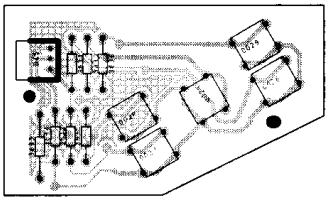


Top control panel / Obere bedienungsplatine / Platine supérieure de commande

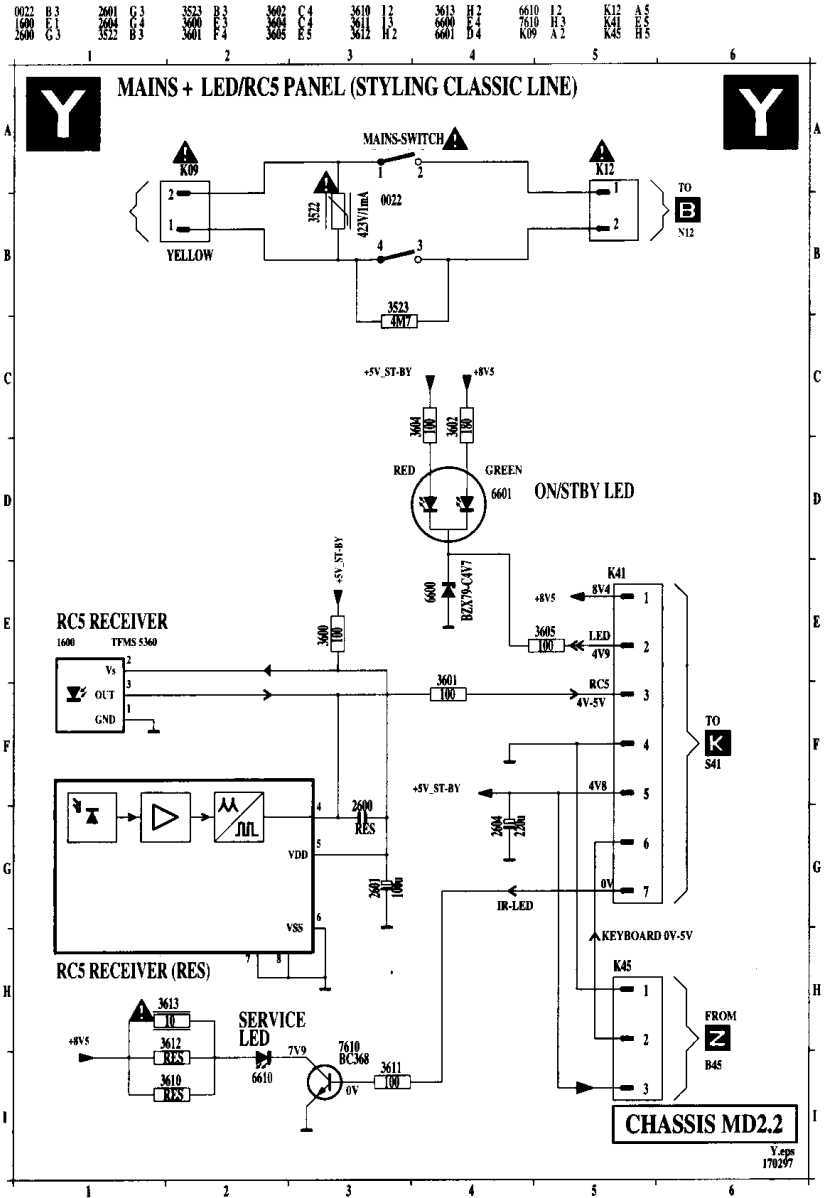


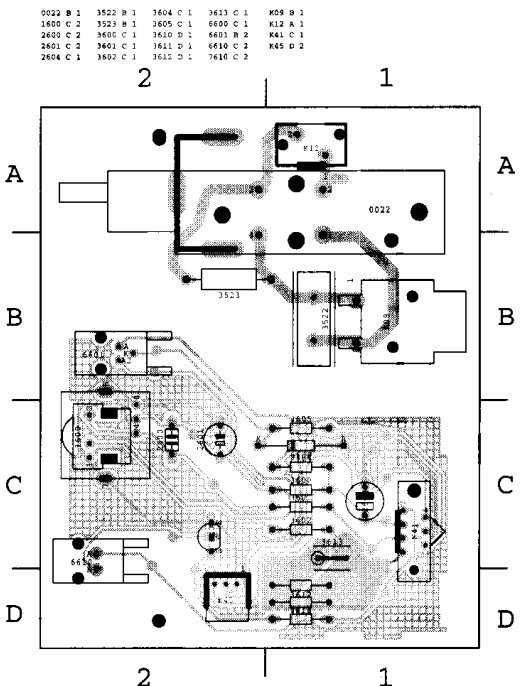




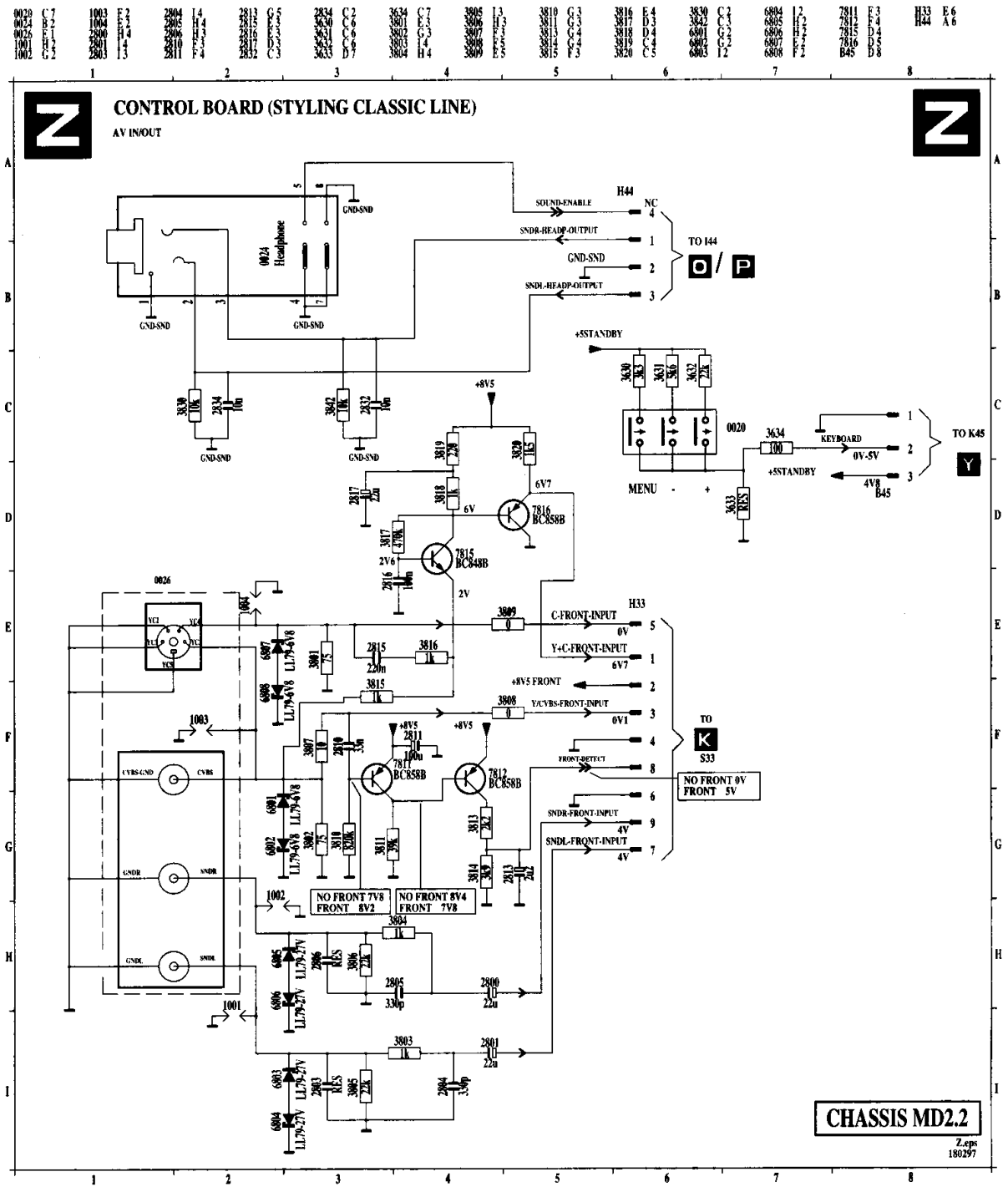


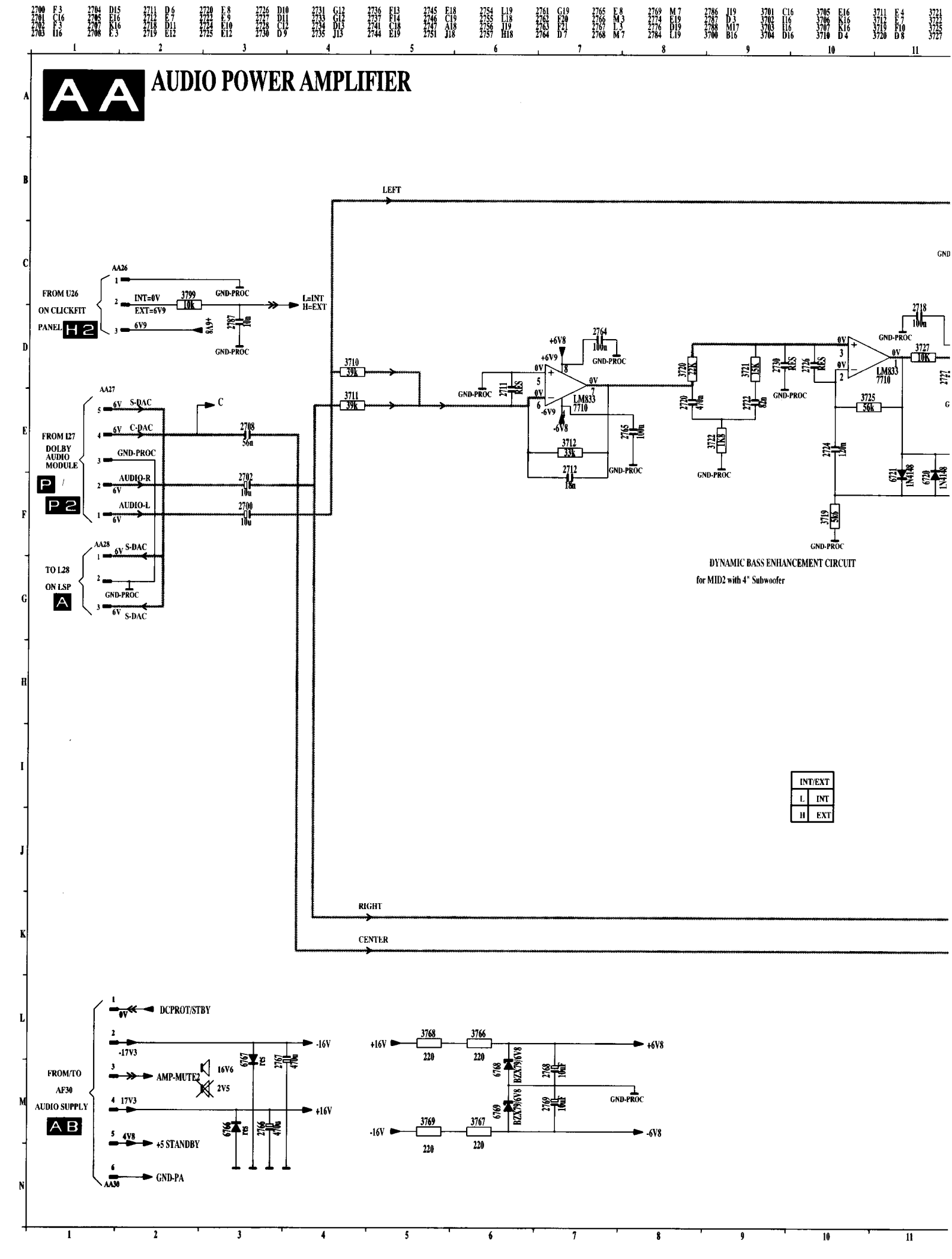
Mains input panel (classic line styling) / Netzeingangsplatine (herkömmliche Bedienung) / Platine entrée secteur (style ligne classique)

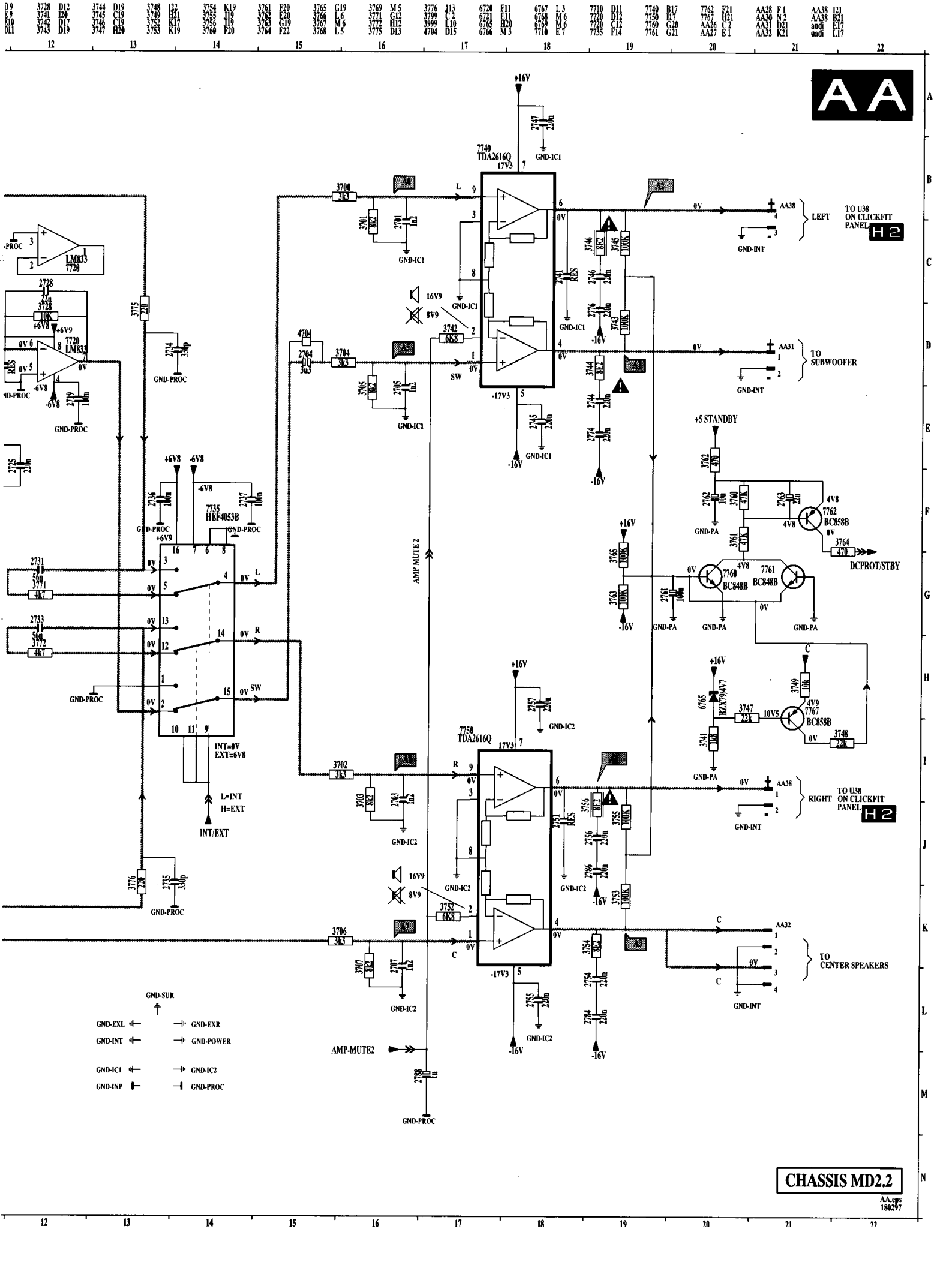




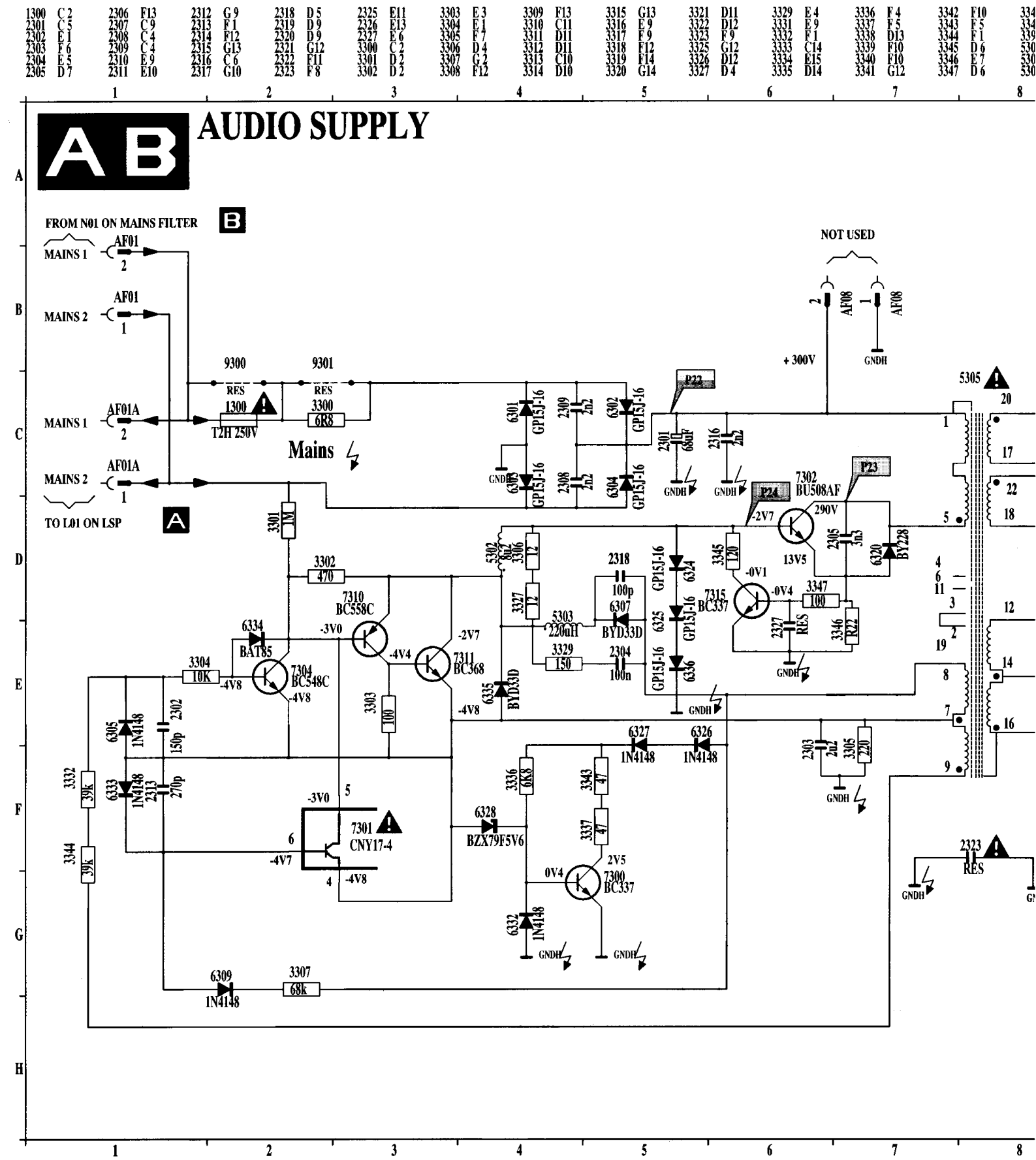
Control board (classic line styling) / Steuerplatine (herkömmliche Bedienung) / Tableau de commande (style ligne classique)




AA AUDIO POWER AMPLIFIER
LEFT
RIGHT
CENTER
FROM U26
ON CLICKFIT
PANEL H2
L=INT
H=EXT
INT=0V
EXT=6V9
FROM I27
DOLBY
AUDIO
MODULE
P / P2
S-DAC
C-DAC
AUDIO-R
AUDIO-L
TO L28
ON LSP
A
LM833
7710
DYNAMIC BASS ENHANCEMENT CIRCUIT
for MID2 with 4" Subwoofer
INT/EXT
L INT
H EXT
FROM/TO
AF30
AUDIO SUPPLY
AB
DCPROT/STBY
AMP-MUTE2
+5 STANDBY
GND-PA
GND-PROC


AA
7740
TDA2616Q
7750
TDA2616Q
LM833
7720
7735
HEF4053B
INT=0V
EXT=6V8
L=INT
H=EXT
INT/EXT
AMP MUTE 2
AMP-MUTE2
LEFT
TO U38 ON CLICKFIT PANEL
H2
TO SUBWOOFER
+5 STANDBY
DCPROT/STBY
RIGHT
TO CENTER SPEAKERS
GND-SUR
GND-EXL
GND-EXR
GND-INT
GND-POWER
GND-IC1
GND-IC2
GND-INP
GND-PROC
CHASSIS MD2.2
AA.eps
180297

Audio supply panel / Ton-Speiseplatine /



Platine alimentation audio

8	D12	5319	F14	6302	C5	6309	G2	6315	F8	6321	F9	6327	E5	6333	F1	7301	F3	7306	F11	9300	B2	AF06	E15								
9	C9	5320	G14	6303	C4	6310	C9	6316	D14	6322	E9	6328	F4	6334	E2	7301	E10	7310	D3	9301	B2	AF08	B7								
8	H8	5333	C14	6304	C5	6311	D10	6317	G11	6323	F11	6329	C10	6335	E4	7302	C6	7311	E3	AF01	B1	AF08	B7								
2	D4	5334	E15	6305	E1	6312	D9	6318	D11	6324	D5	6330	E13	6336	E5	7303	D11	7312	G12	AF01	A1	AF30	C15								
3	E4	5335	D14	6307	D5	6313	E9	6319	G10	6325	D5	6331	F12	6337	E9	7304	E2	7314	E12	AF01AC1		k1	B8								
5	C8	6301	C4	6308	F11	6314	E9	6320	D7	6326	E5	6332	G4	7300	G5	7305	F10	7315	D6	AF01AC1		k3	B7								

9 10 11 12 13 14 15

AUDIO SUPPLY AB

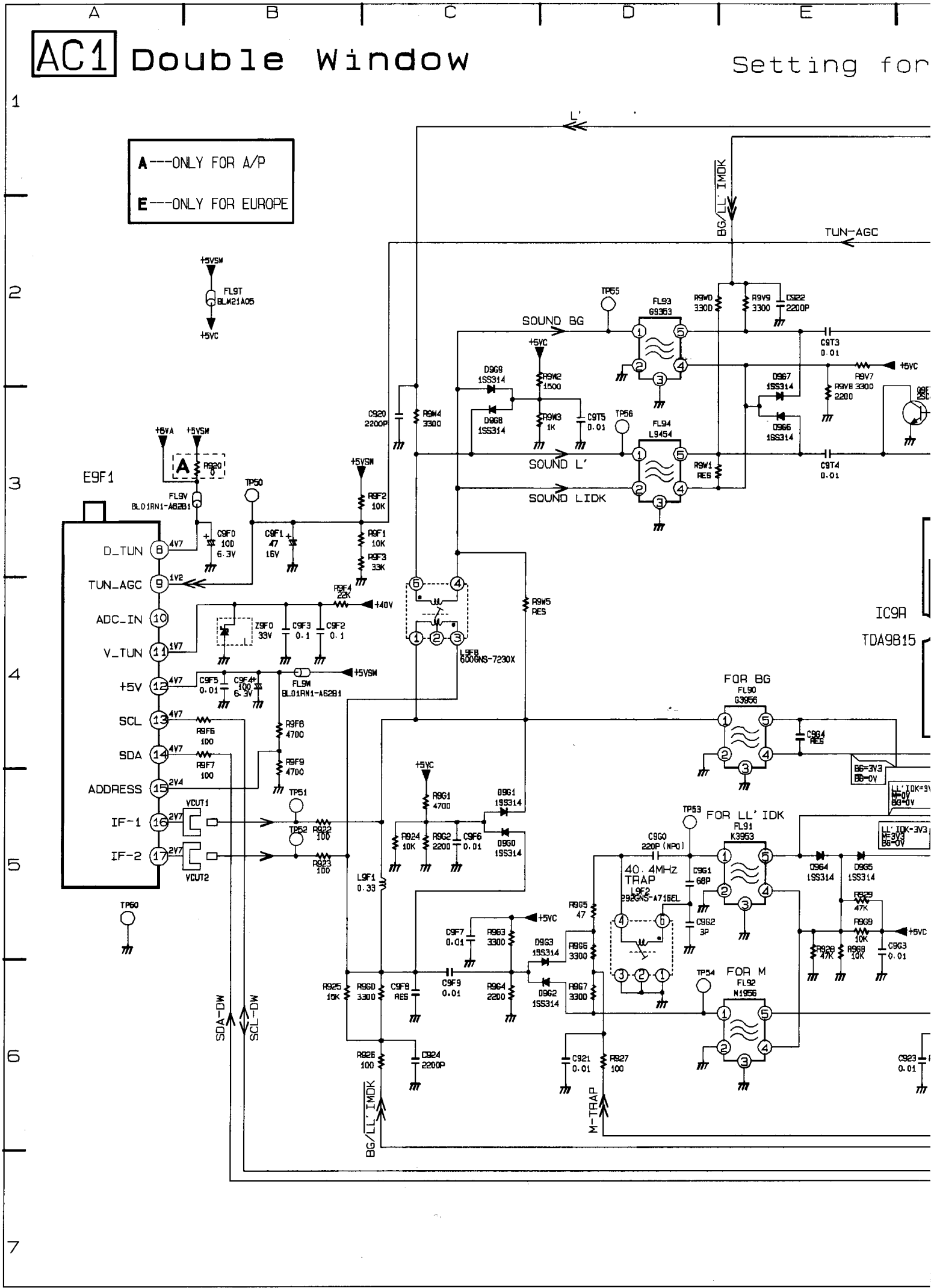
TO AA30 ON AUDIO AMPLIFIER PANEL AA

FROM L06 LARGE SIGNAL PANEL A

(...V) MEASURED IN

CHASSIS MD2.2

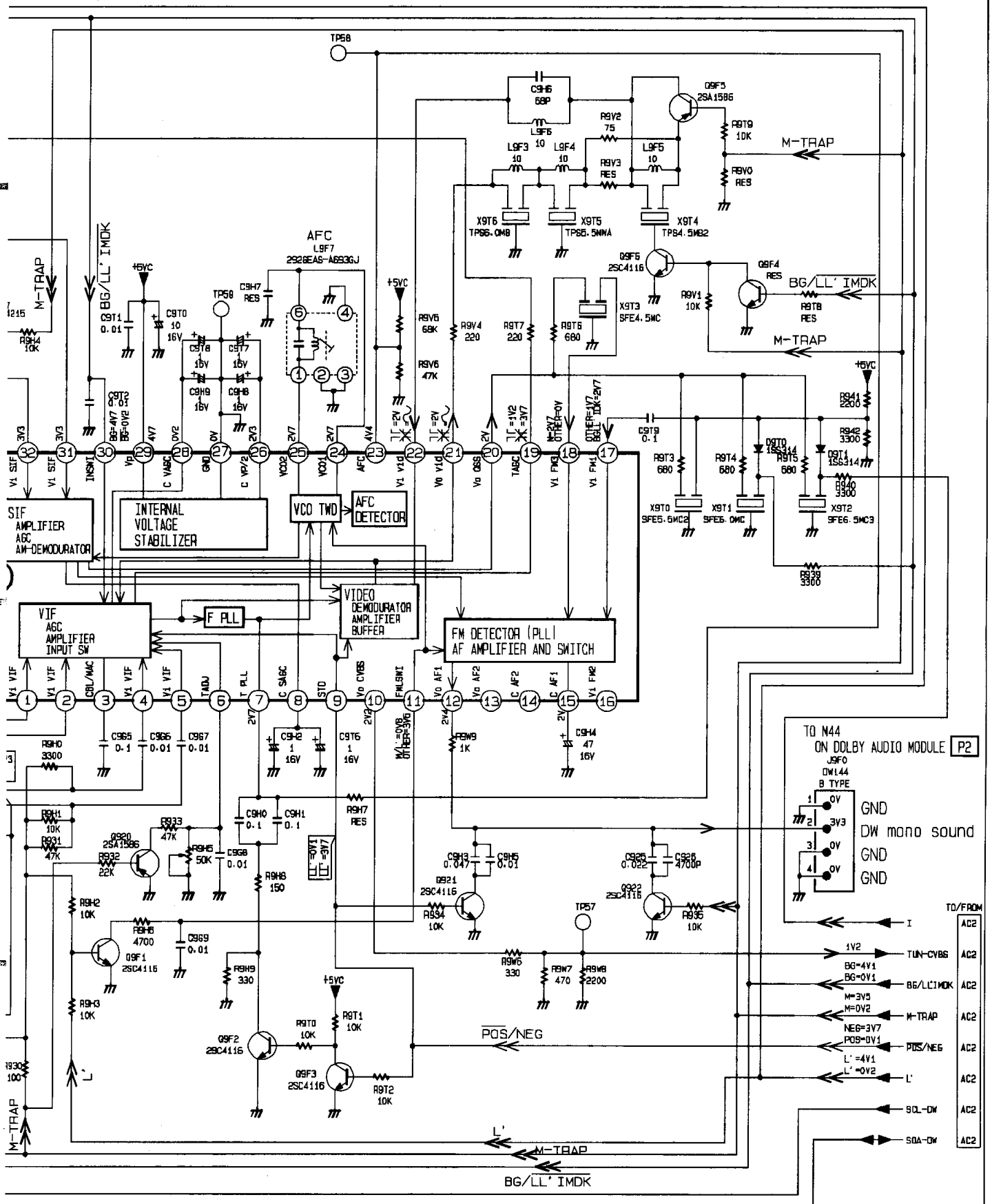
AB.eps 180297

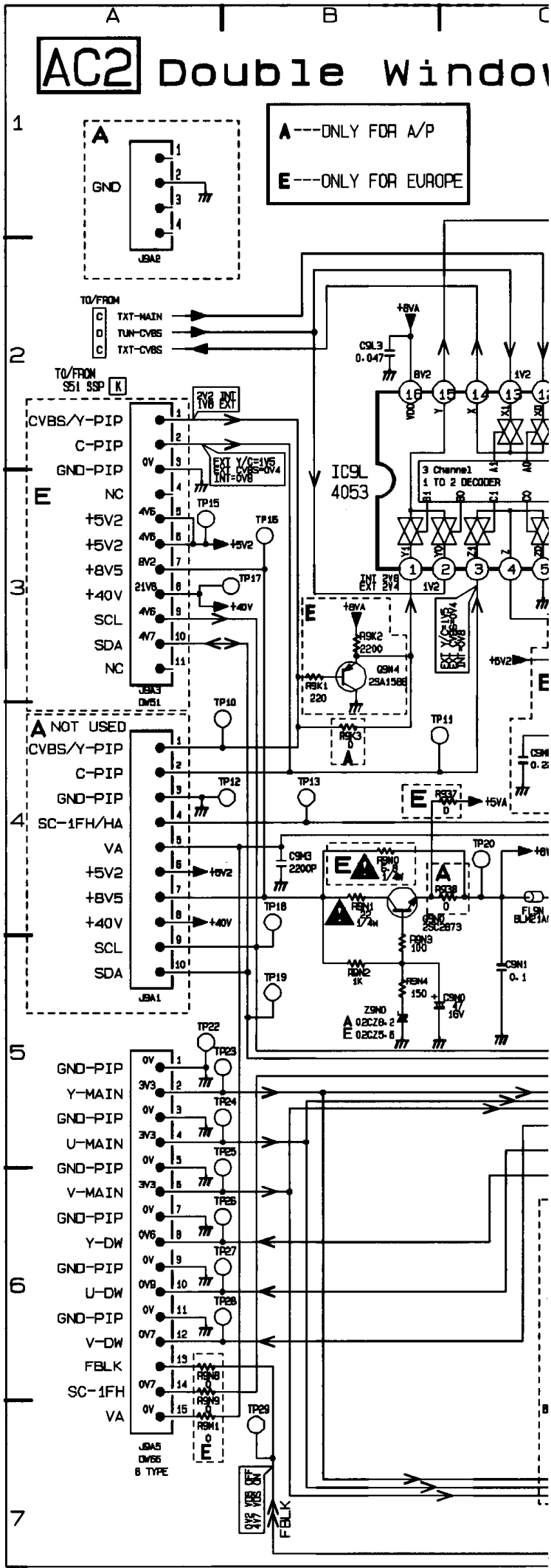

AC1 Double Window
Setting for
A---ONLY FOR A/P
E---ONLY FOR EUROPE
E9F1
D_TUN
TUN_AGC
ADC_IN
V_TUN
+5V
SCL
SDA
ADDRESS
IF-1
IF-2
VCUT1
VCUT2
TP50
TP51
TP52
TP53
TP54
TP55
TP56
TP60
+5VSW
+5VC
+5VA
+40V
BG/LL'IMDK
TUN-AGC
SOUND BG
SOUND L'
SOUND LIDK
SDA-DW
SCL-DW
M-TRAP
IC9A
TDA9815
FOR BG
FOR LL' IDK
FOR M
40.4MHz TRAP

F G H I J

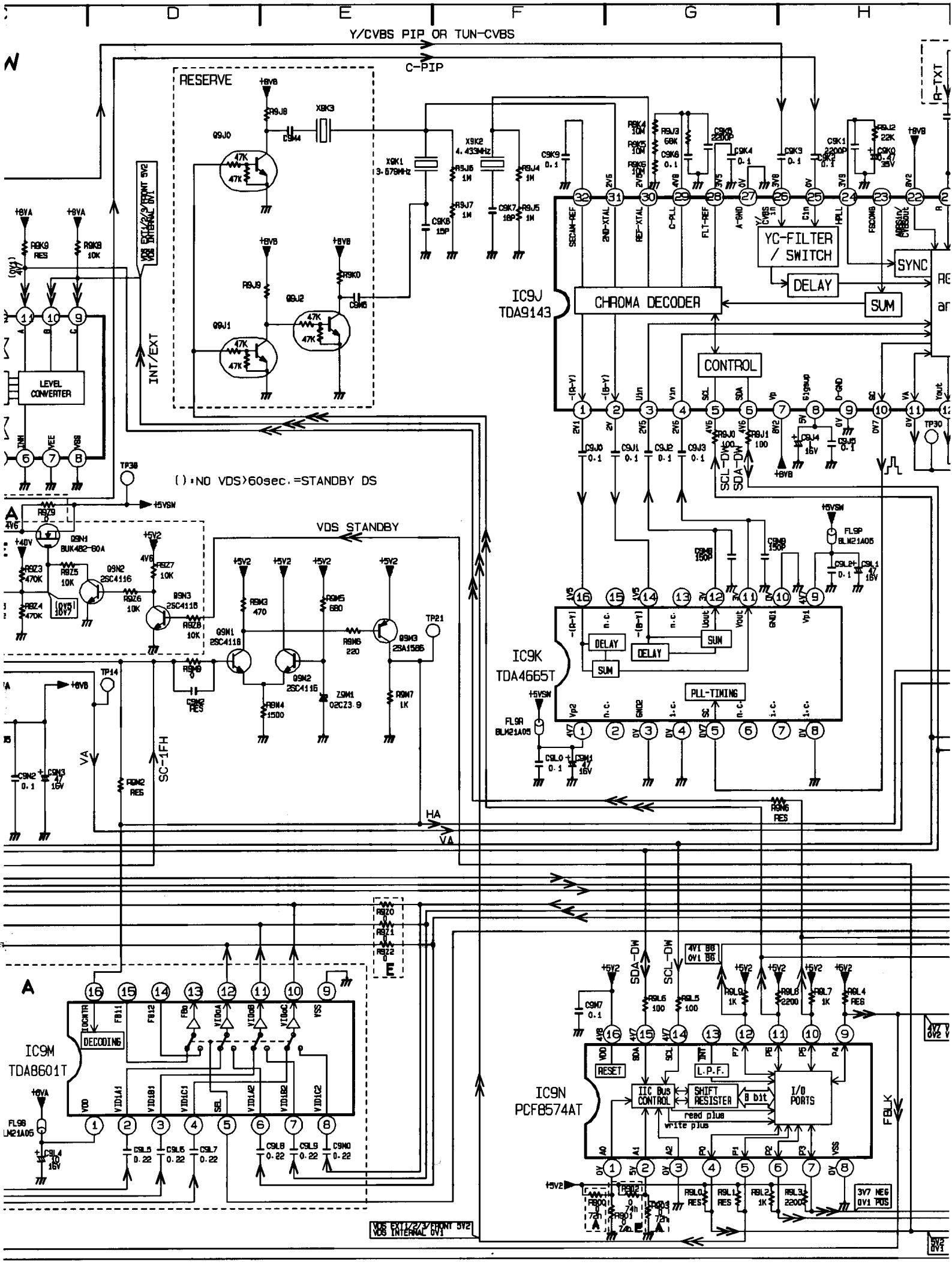
measurments : SDM+VDS picture mode

AC1

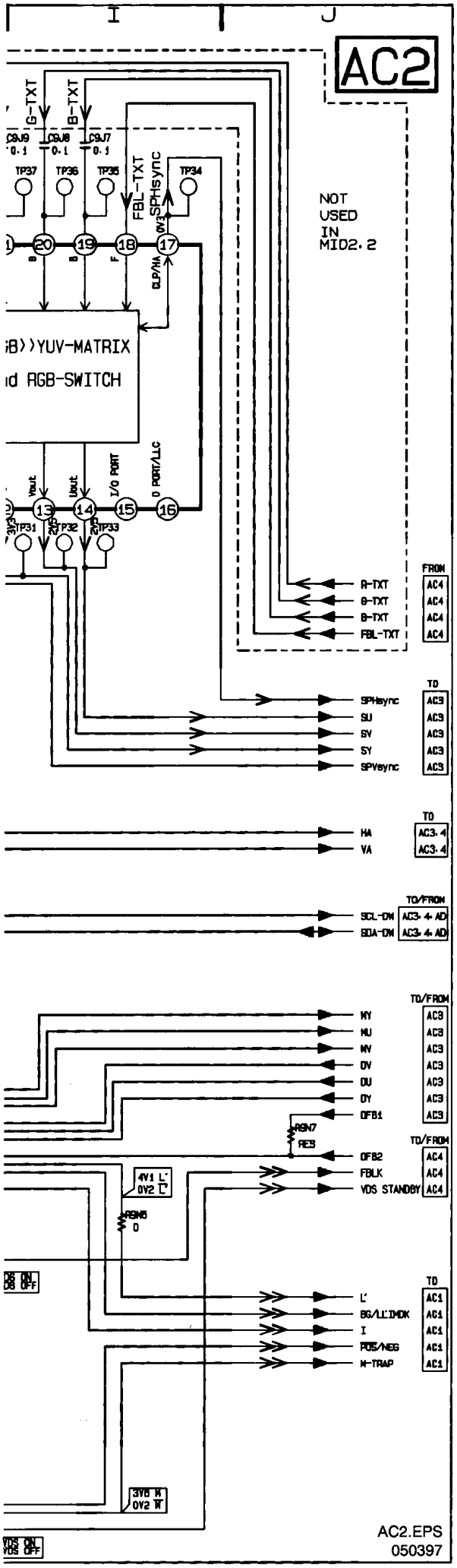



AC2 Double Windo
A---ONLY FOR A/P
E---ONLY FOR EUROPE
GND
TO/FROM
TXT-MAIN
TUN-CVBS
TXT-CVBS
TO/FROM SS1 SSP
CVBS/Y-PIP
C-PIP
GND-PIP
NC
+5V2
+5V2
+8V5
+40V
SCL
SDA
NC
NOT USED
CVBS/Y-PIP
C-PIP
GND-PIP
SC-1FH/HA
VA
+5V2
+8V5
+40V
SCL
SDA
GND-PIP
Y-MAIN
GND-PIP
U-MAIN
GND-PIP
V-MAIN
GND-PIP
Y-DW
GND-PIP
U-DW
GND-PIP
V-DW
FBLK
SC-1FH
VA
IC9L
4053
3 Channel
1 TO 2 DECODER
+8VA
+5V2
+40V
+5VA
FBLK

Video-DualScreen-Platine / Platine Video DualScreen



Video DualScreen panel /



PIN2 IC9L
0.5V / div AC
20µs / div

TP31
0.5V / div DC
20µs / div

TP30 11-9143
1V / div AC
10ms / div

PIN26 IC9J
0.2V / div AC
20µs / div

TP32
0.5V / div DC
20µs / div

TP34 17-9143
1V / div AC
20µs / div

PIN1 IC9J
0.1V / div AC
20µs / div

TP33
0.5V / div DC
20µs / div

Pin93 IC9A 2-IC4053
1V / div AC
20µs / div

PIN2 IC9J
0.1V / div AC
20µs / div

TP01 6-8601
0.2V / div AC
20µs / div

TP14 5-P51
1V / div AC
10ms / div

PIN3 IC9J
0.2V / div AC
20µs / div

TP02 7-8601
0.2V / div AC
20µs / div

TP21 4-P51
0.5V / div AC
20µs / div

PIN4 IC9J
0.2V / div AC
20µs / div

TP03 8-8601
0.2V / div AC
20µs / div

TP26
0.2V / div AC
20µs / div

TP24
0.2V / div AC
20µs / div

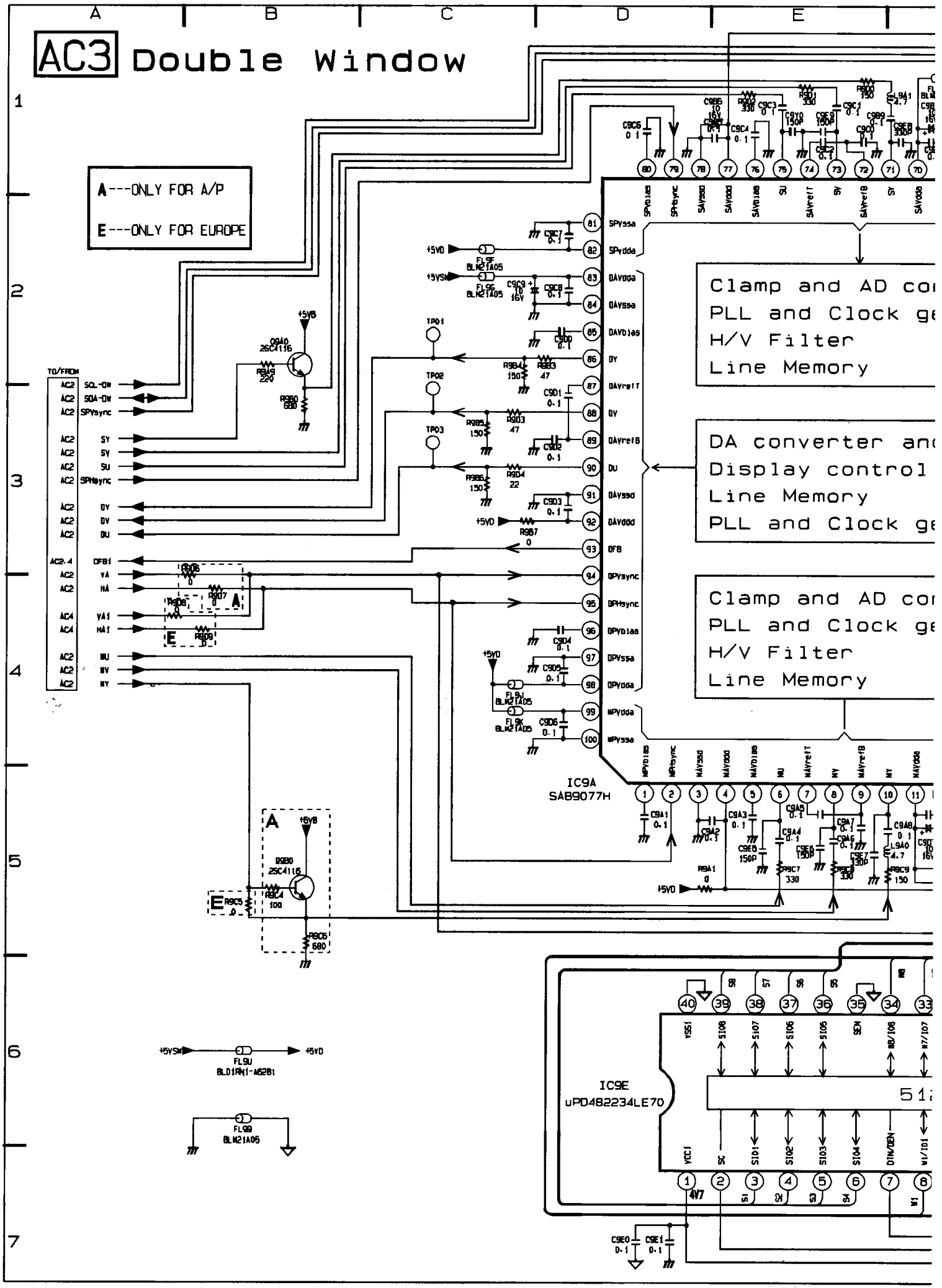
TP27
0.2V / div AC
20µs / div

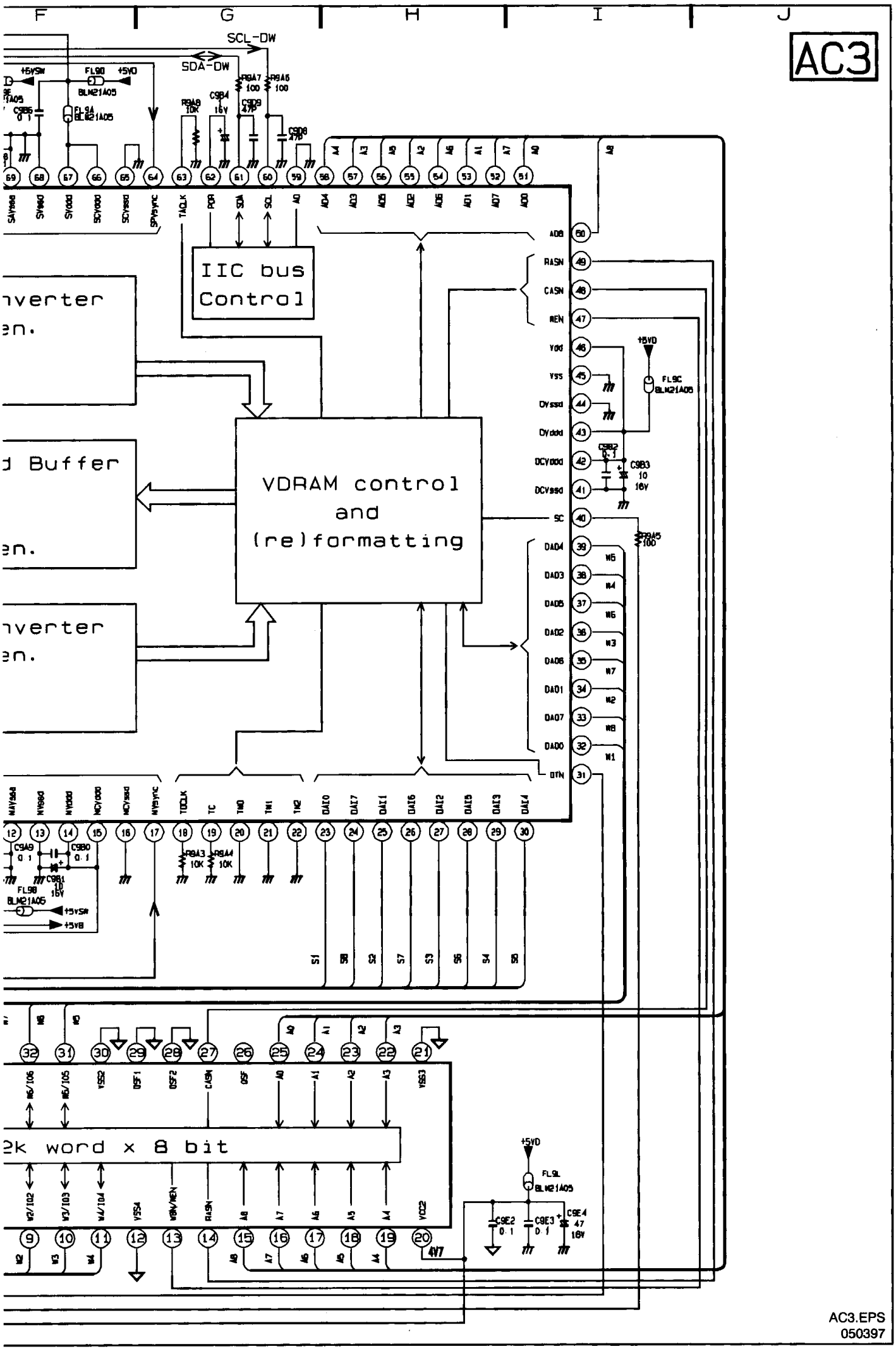
TP25
0.2V / div AC
20µs / div

TP28
0.2V / div AC
20µs / div

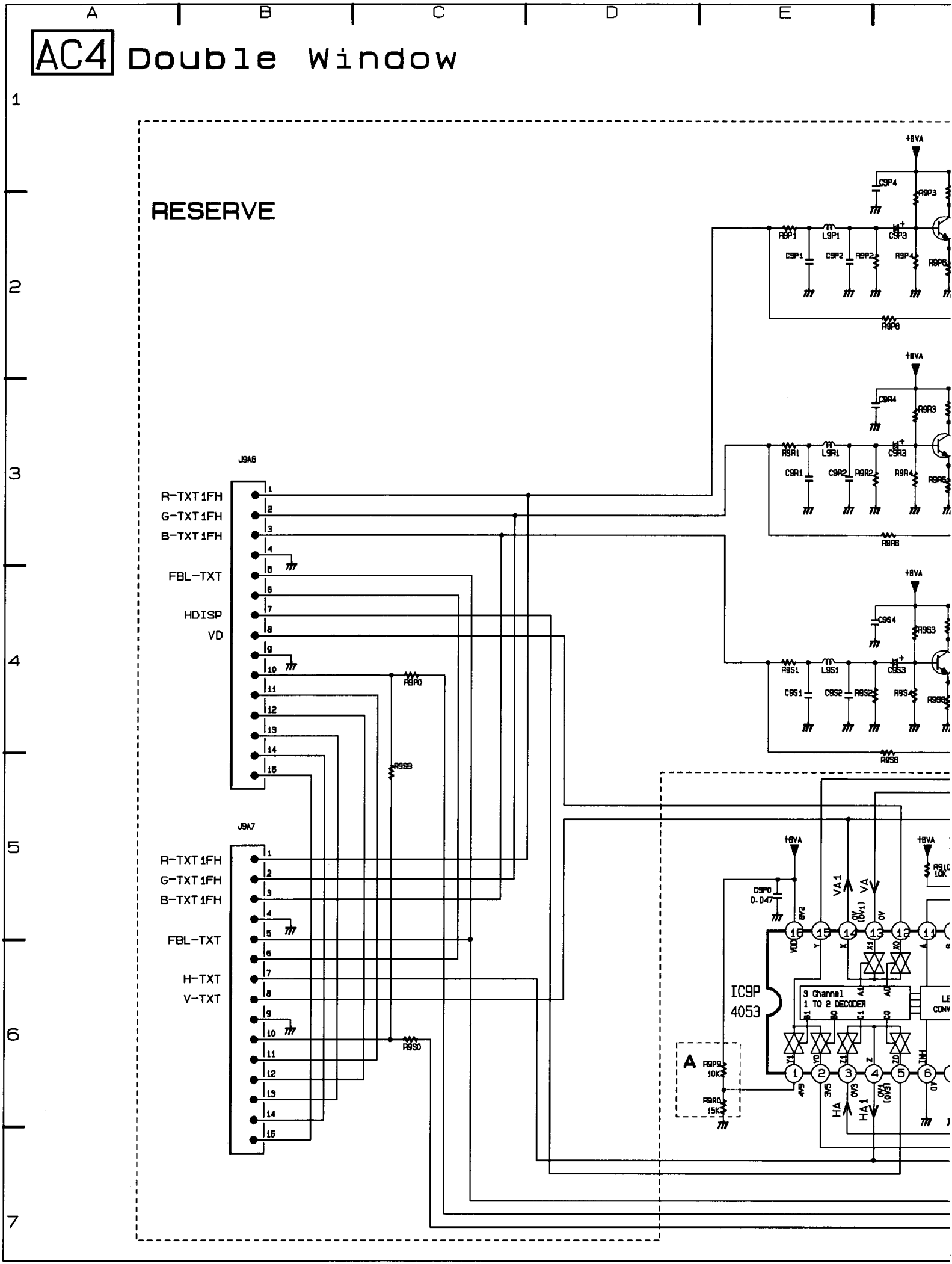
TP23
0.2V / div AC
20µs / div

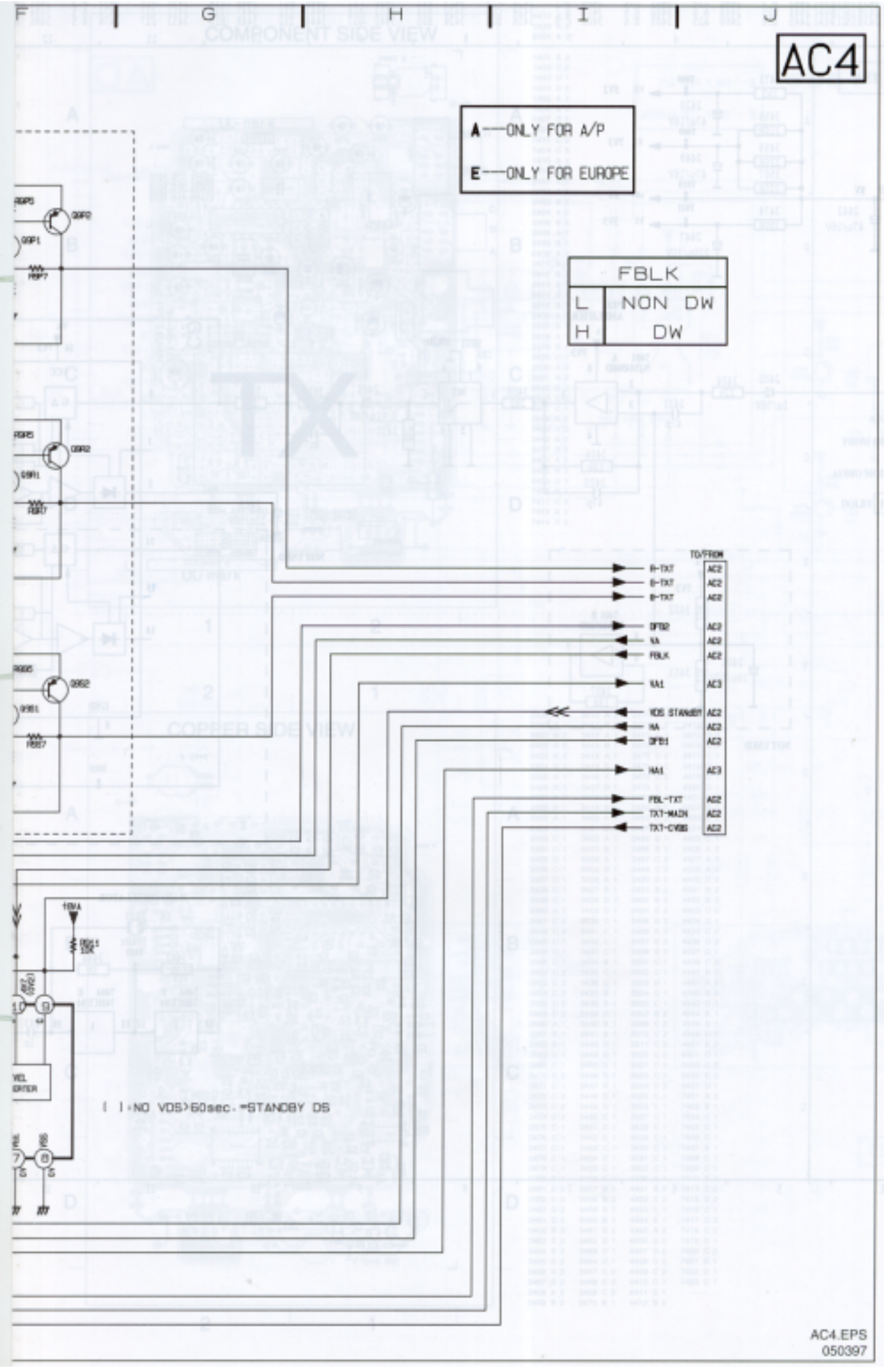
OSC_AC1-2.AI
050397


AC3 Double Window
A---ONLY FOR A/P
E---ONLY FOR EUROPE
Clamp and AD co
PLL and Clock ge
H/V Filter
Line Memory
DA converter an
Display control
Line Memory
PLL and Clock ge
Clamp and AD co
PLL and Clock ge
H/V Filter
Line Memory
IC9A
SAB9077H
IC9E
uPD482234LE70
TO/FROM

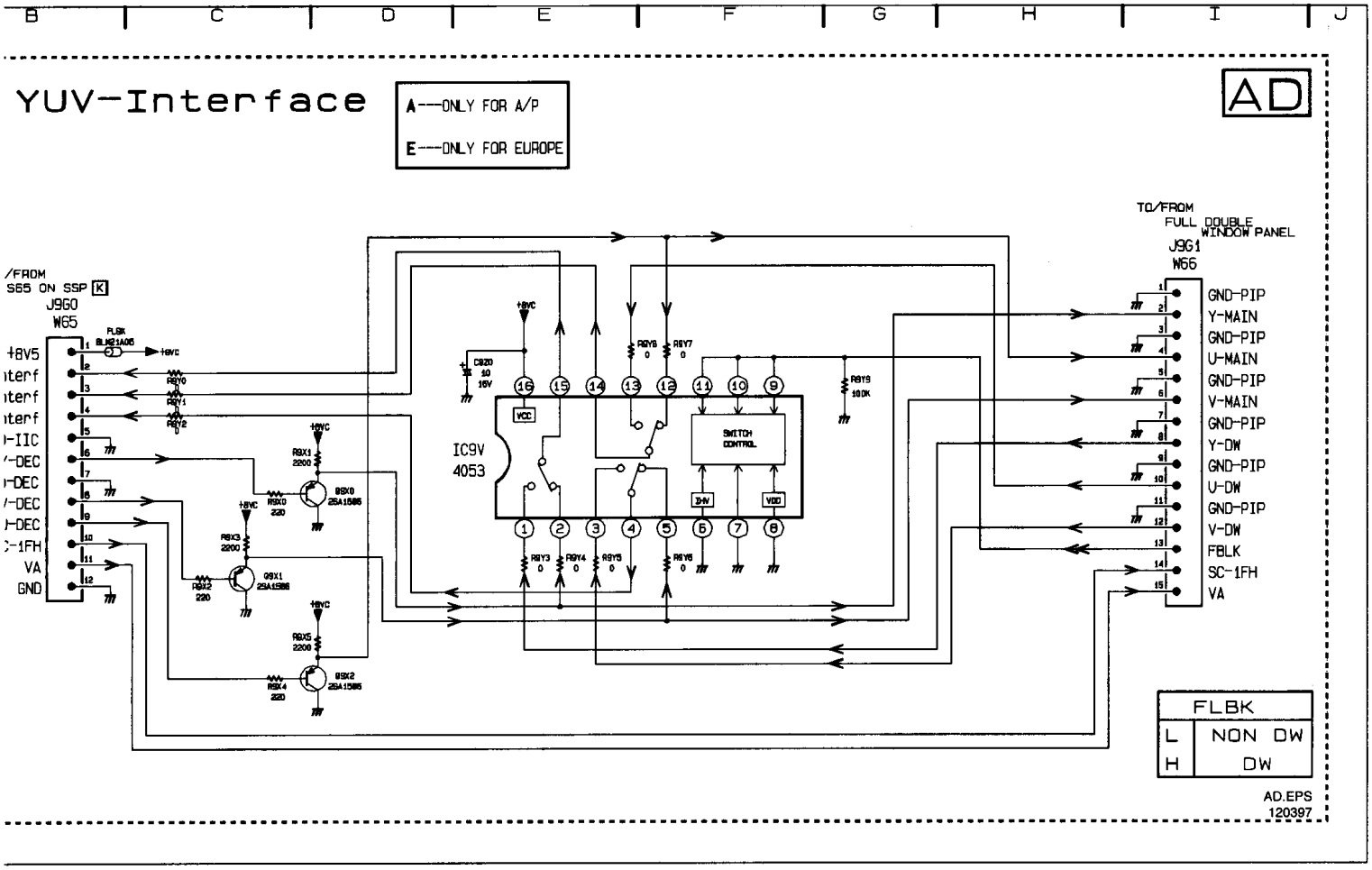

AC3
SCL-DW
SDA-DW
IIC bus Control
VDRAM control and (re)formatting
Buffer
2k word x 8 bit
AC3.EPS
050397

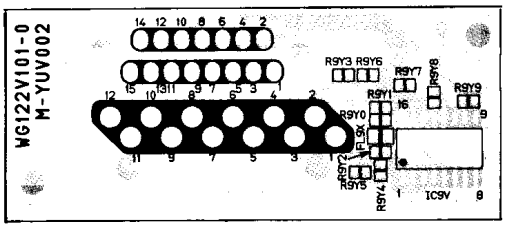
Video DualScreen panel / Video-DualScreen-Platine / Platine Video DualScreen

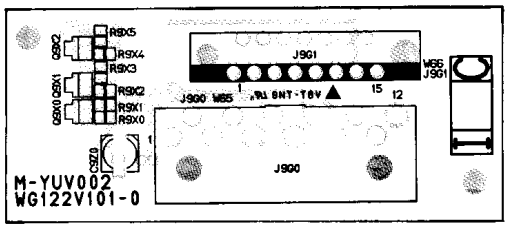


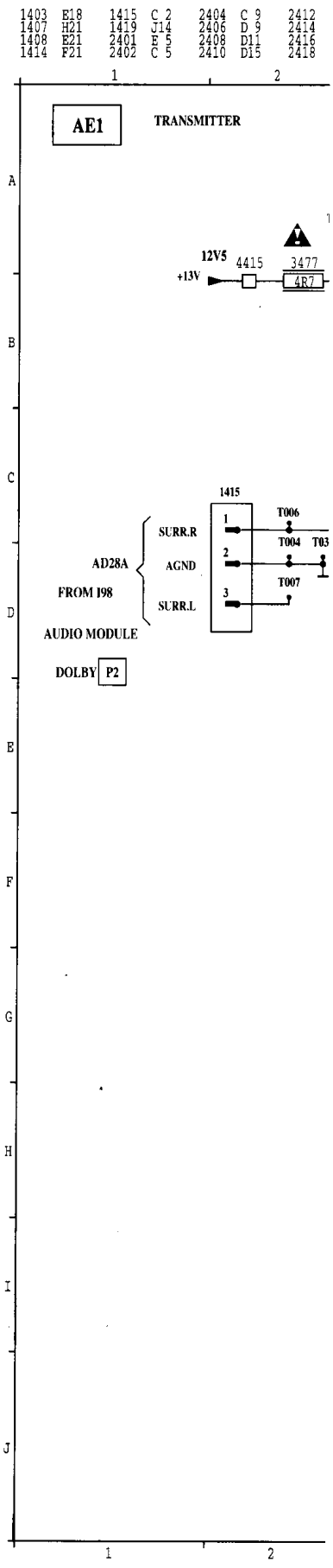

AC4
A---ONLY FOR A/P
E---ONLY FOR EUROPE
FBLK
L NON DW
H DW
TO/FROM
B-TXT AC2
B-TXT AC2
B-TXT AC2
DFB2 AC2
NA AC2
FBLK AC2
NA1 AC3
VDS STANDBY AC2
NA AC2
DFB1 AC2
NA1 AC3
FBL-TXT AC2
TXT-MAIN AC2
TXT-CVBS AC2
( )-NO VDS>60sec.=STANDBY DS
AC4.EPS
050397

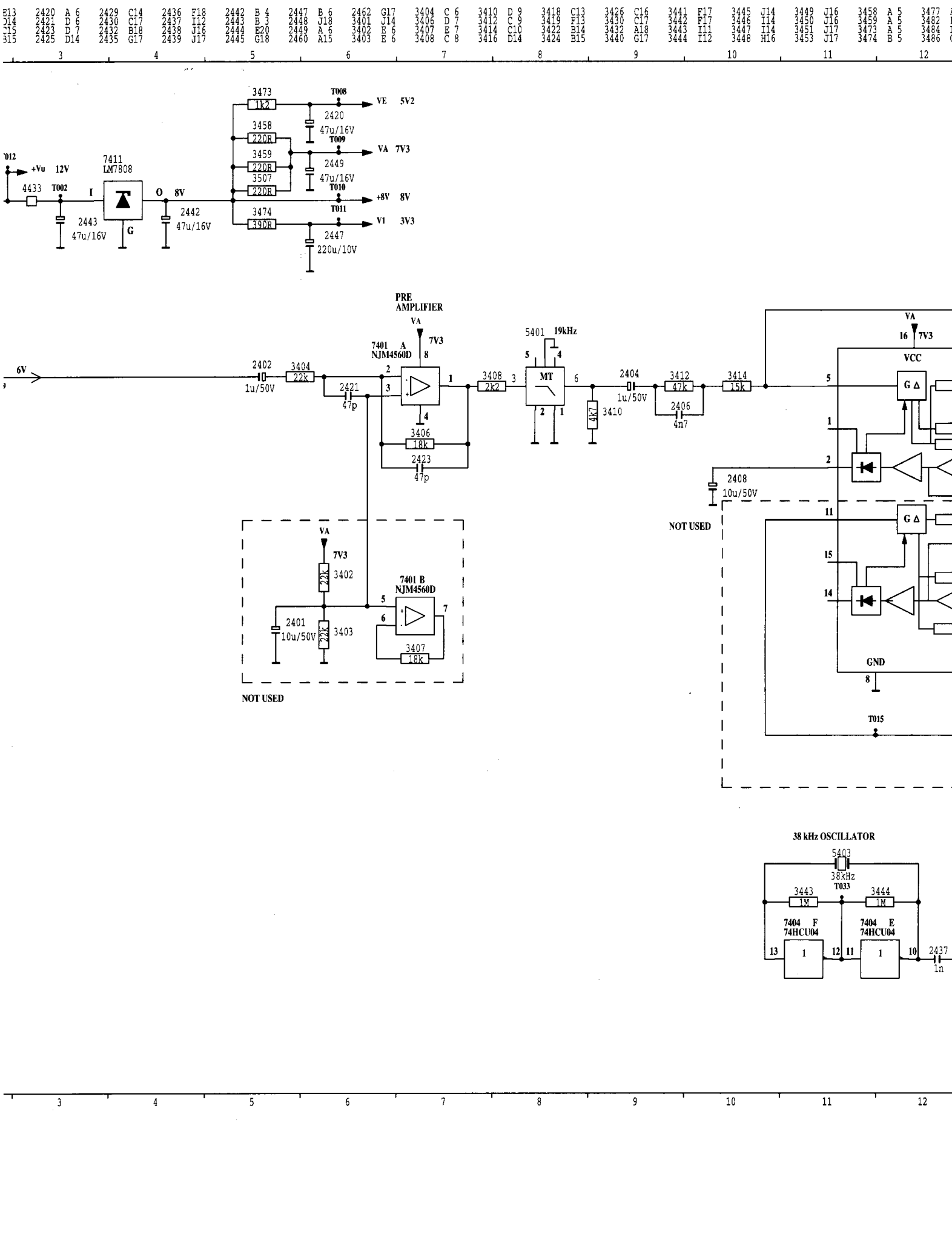
YUV-interface panel / YUV-Schnittstellenplatine / Platine YUV-interface








1403 E18
1407 H21
1408 E21
1414 F21
1415 C 2
1419 J14
2401 E 5
2402 C 5
2404 C 9
2406 D 9
2408 D11
2410 D15
2412
2414
2416
2418
1
2
AE1
TRANSMITTER
A
B
C
D
E
F
G
H
I
J
12V5
+13V
4415
3477
4R7
1415
1
2
3
T006
T004
T03
T007
SURR.R
AGND
SURR.L
AD28A
FROM I98
AUDIO MODULE
DOLBY
P2


3473
1k2
T008
VE 5V2
2420
47u/16V
3458
220R
3459
220R
3507
220R
T009
VA 7V3
2449
47u/16V
T010
+8V 8V
3474
390R
T011
V1 3V3
2447
220u/10V
+Vu 12V
7411
LM7808
4433
T002
I
O 8V
2443
47u/16V
G
2442
47u/16V
PRE
AMPLIFIER
VA
7401 A
NJM4560D
7V3
6V
2402
1u/50V
3404
22k
2421
47p
3406
18k
2423
47p
3408
2k2
5401 19kHz
MT
2404
1u/50V
3410
4k7
3412
47k
2406
4n7
3414
15k
VA
16 7V3
VCC
G Δ
2408
10u/50V
NOT USED
7401 B
NJM4560D
3402
22k
2401
10u/50V
3403
22k
3407
18k
NOT USED
GND
T015
38 kHz OSCILLATOR
5403
38kHz
T033
3443
1M
3444
1M
7404 F
74HCU04
7404 E
74HCU04
2437
1n

Wireless Dolby / Drahtlos-Dolby / Dolby sans fil

2	3501	H19	3505	G20	4415	A 2	5401	C 8	7401	E 7	7404	B18	7404	I11	7410	G17
16	3502	H20	3507	A 5	4430	I20	5403	H11	7402	F14	7404	I17	7404	I11	7411	A 3
14	3503	G21	4400	C16	4433	A 3	6401	I14	7402	B15	7404	I16	7405	I15		
17	3504	H21	4405	C17	4445	I20	7401	C 6	7403	C13	7404	I15	7406	I17		

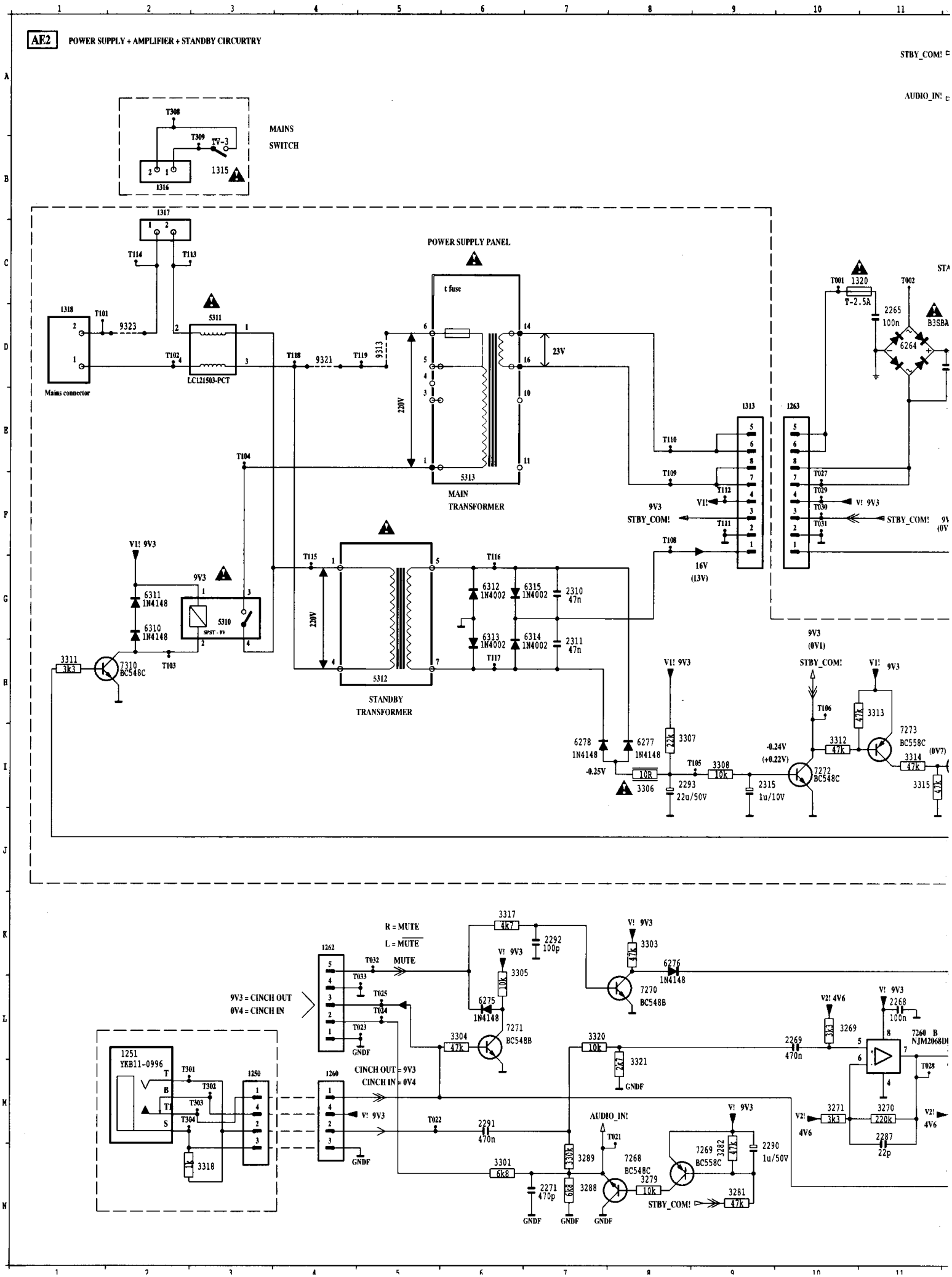
13 14 15 16 17 18 19 20 21

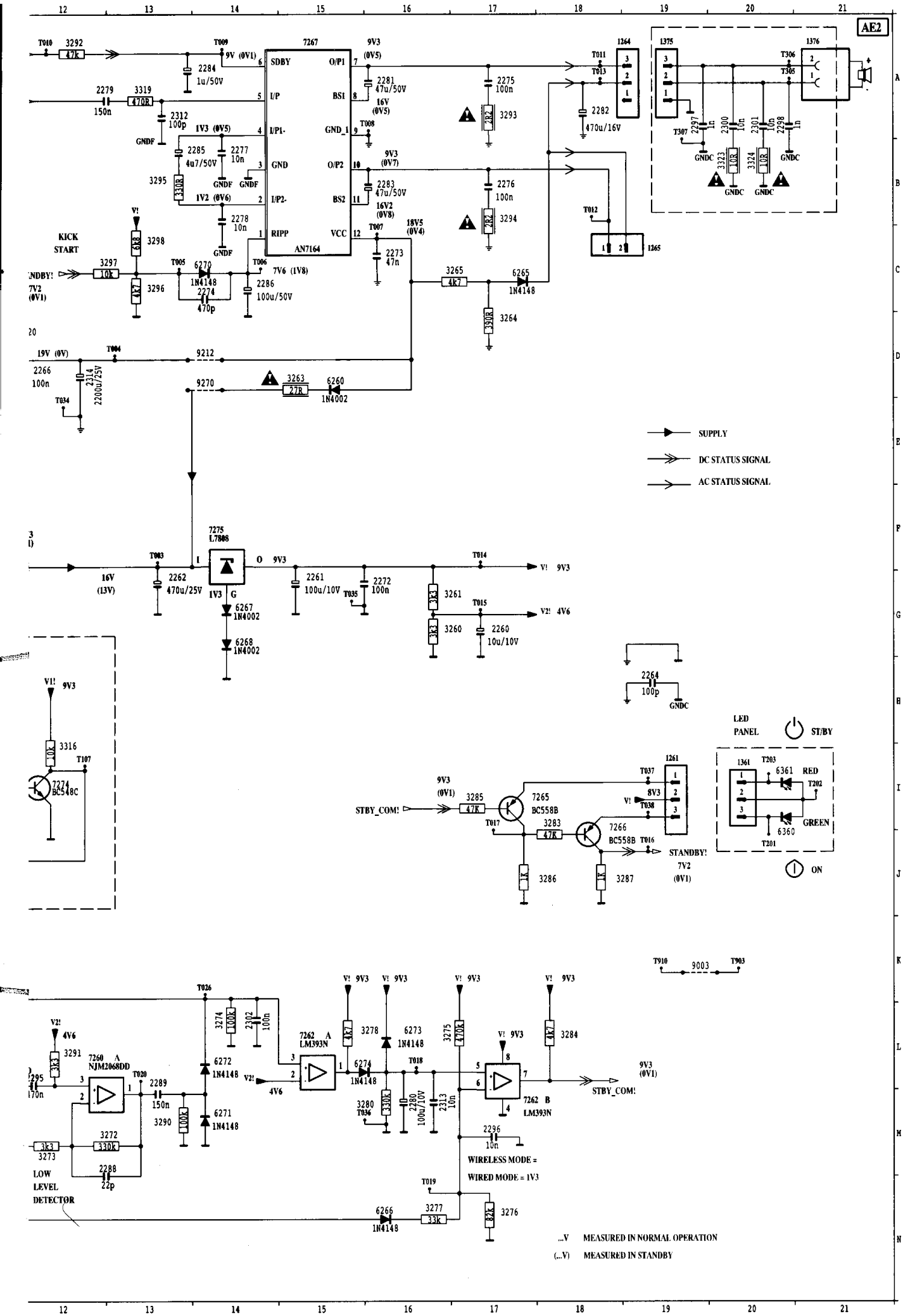
TRANSMITTER **AE1**

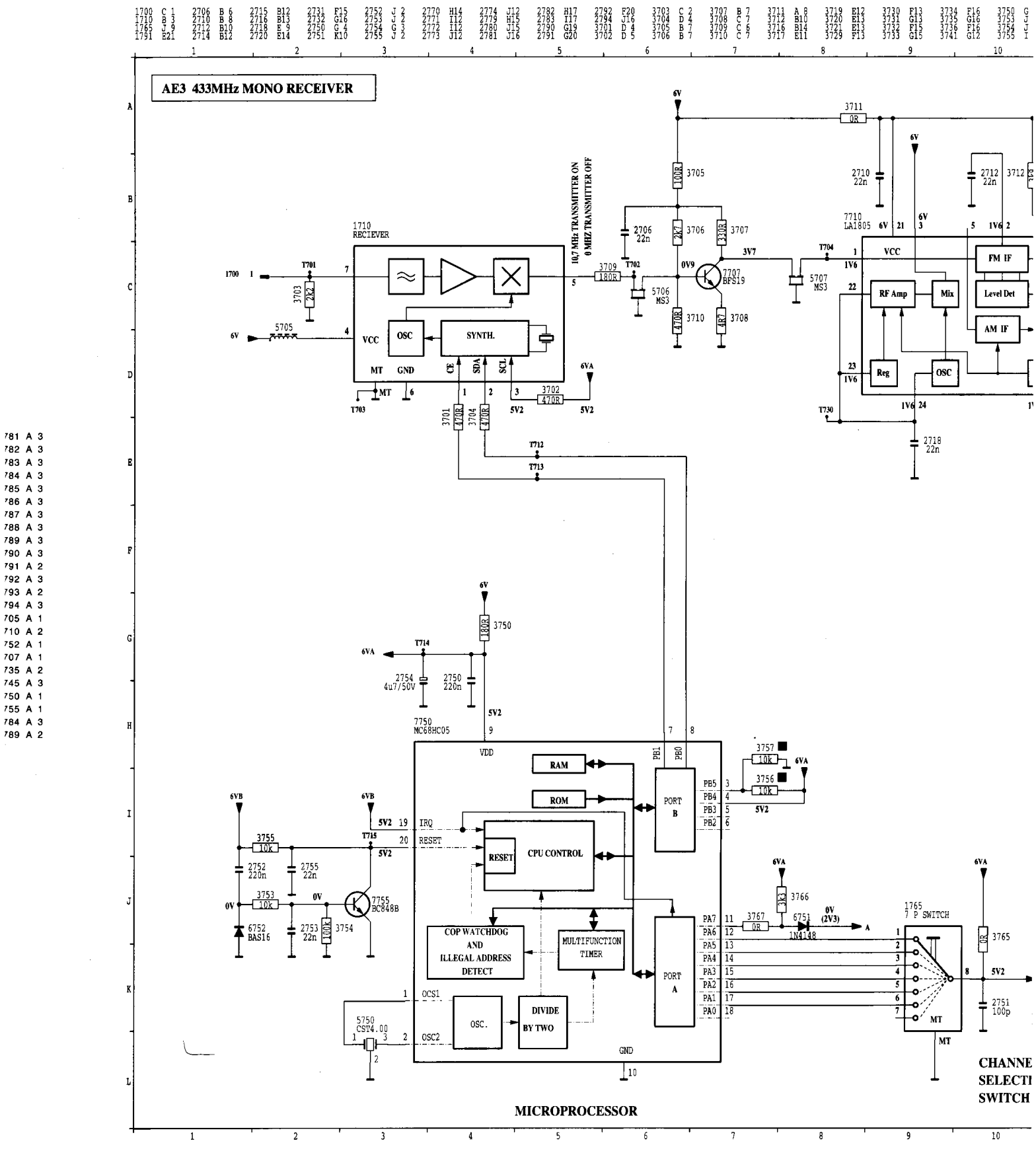
COMPANDER

2460 47p
3422 18k
3424 18k
2418 10u/50V
7402 B NJM4560D
3432 56k
2432 47p
V1
3V3
7404 A 74HCU04 14
4400 chip jumper
3426 1k
4405 chip jumper
T014
2430 1u/50V
3430 47k
7403 NE572
2429 47p
2416 2u2/50V
3418 1k
2414 2u2/50V
3484 10k
3416 3k3
2425 22n
2410 2u2/50V
2412 470n
3419 1k
7402 A NJM4560D
VA 7V3
+8V
2444 100p
1403 TRANSMITTER
8v
VCC
ANTENNA
T035 1408 1
0v
T036 1414 1
OSC
SYNTH.
SCL SDA CE GND
MT
VE
5V2
3442 1k
T034
3482 33k
3441 100k
3V
1V7
7410 BC847B
3440 10k
2462 100p
1V
2435 180p
470R 3486
6V1
2436 470n
2445 47p
4v7 4v7 4v2
+Vu
T017 T018
470R 3505
8k2 3503
3501 470R
3502 470R
4k7 3504
T022
1407
+13V
12v5
T037 T021
T020 4430
T019 4445
T040 4v7
4v7
+13V
GND
SDA
SCL
AD99 FROM I99 AUDIO MODULE DOLBY P2
2 DIVIDER
3448 100k
7404 D 74HCU04
7404 C 74HCU04
7404 B 74HCU04
3447 10k
6401 BAS16
3446 10k
7405 BC847B
19kHz
10k
3449
3450 100k
7406 BC847B
V1
3v3
1v6
1v
3451 27k
2448 5n6
4k7 3445
3401 470R
NOT USED
1419
2438 1n
2439 100p
4k7 3453

CHASSIS MD2.2


AE2
POWER SUPPLY + AMPLIFIER + STANDBY CIRCURTRY
MAINS SWITCH
POWER SUPPLY PANEL
t fuse
MAIN TRANSFORMER
STANDBY TRANSFORMER
Mains connector
LC121503-PCT
STBY_COM!
AUDIO_IN!
R = MUTE
L = MUTE
9V3 = CINCH OUT
0V4 = CINCH IN
CINCH OUT = 9V3
CINCH IN = 0V4
YKB11-0996
NJM2068D


AE2
AN7164
7267
7275 L7808
7260 A NJM2068DD
7262 A LM393N
7262 B LM393N
7265 BC558B
7266 BC558B
7274 BC548C
KICK START
LOW LEVEL DETECTOR
LED PANEL
ST/BY
ON
RED
GREEN
STANDBY! 7V2 (0V1)
STBY_COM!
WIRELESS MODE =
WIRED MODE = 1V3
SUPPLY
DC STATUS SIGNAL
AC STATUS SIGNAL
...V MEASURED IN NORMAL OPERATION
(...V) MEASURED IN STANDBY



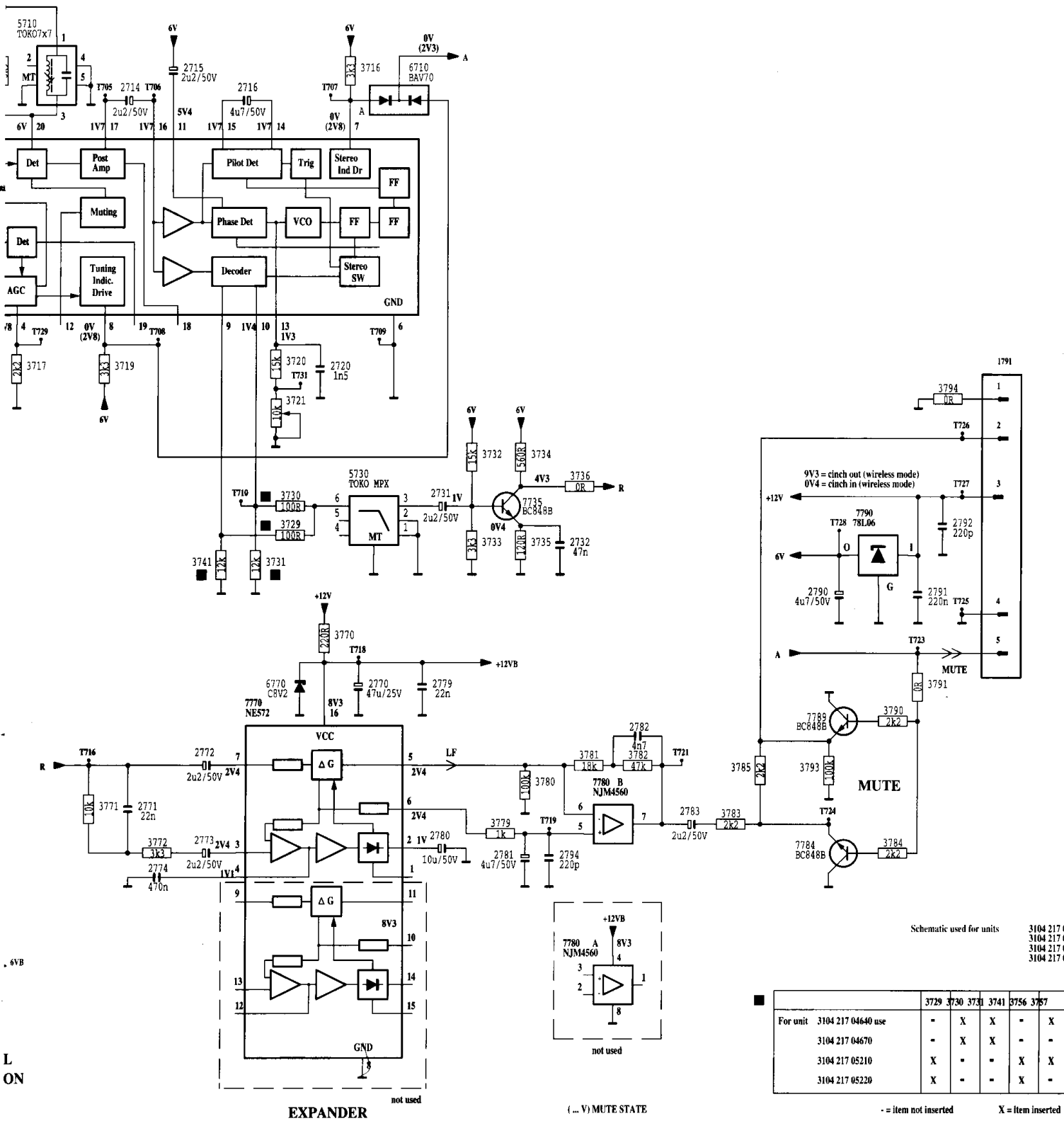
781 A 3
782 A 3
783 A 3
784 A 3
785 A 3
786 A 3
787 A 3
788 A 3
789 A 3
790 A 3
791 A 2
792 A 3
793 A 2
794 A 3
705 A 1
710 A 2
752 A 1
707 A 1
735 A 2
745 A 3
750 A 1
755 A 1
784 A 3
789 A 2

Wireless Dolby / Drahtlos-Dolby / Dolby sans fil

4	3756	I 7	3767	J 7	3779	I16	3783	I18	3791	H20	5706	C 6	5750	K 3	6770	H13	7750	H 3	7780	I16
2	3757	H 7	3770	H14	3780	I16	3784	J20	3793	I19	5707	C 8	6710	B15	7707	C 7	7755	J 3	7784	J19
3	3765	J10	3771	I12	3781	I16	3785	I18	3794	B20	5710	A11	6751	J 8	7710	B 8	7770	H13	7789	H19
2	3766	J 8	3772	J12	3782	I17	3790	H20	5705	C 2	5730	F14	6752	J 2	7735	F16	7780	K16	7790	F19

11 12 13 14 15 16 17 18 19 20 21

AE3



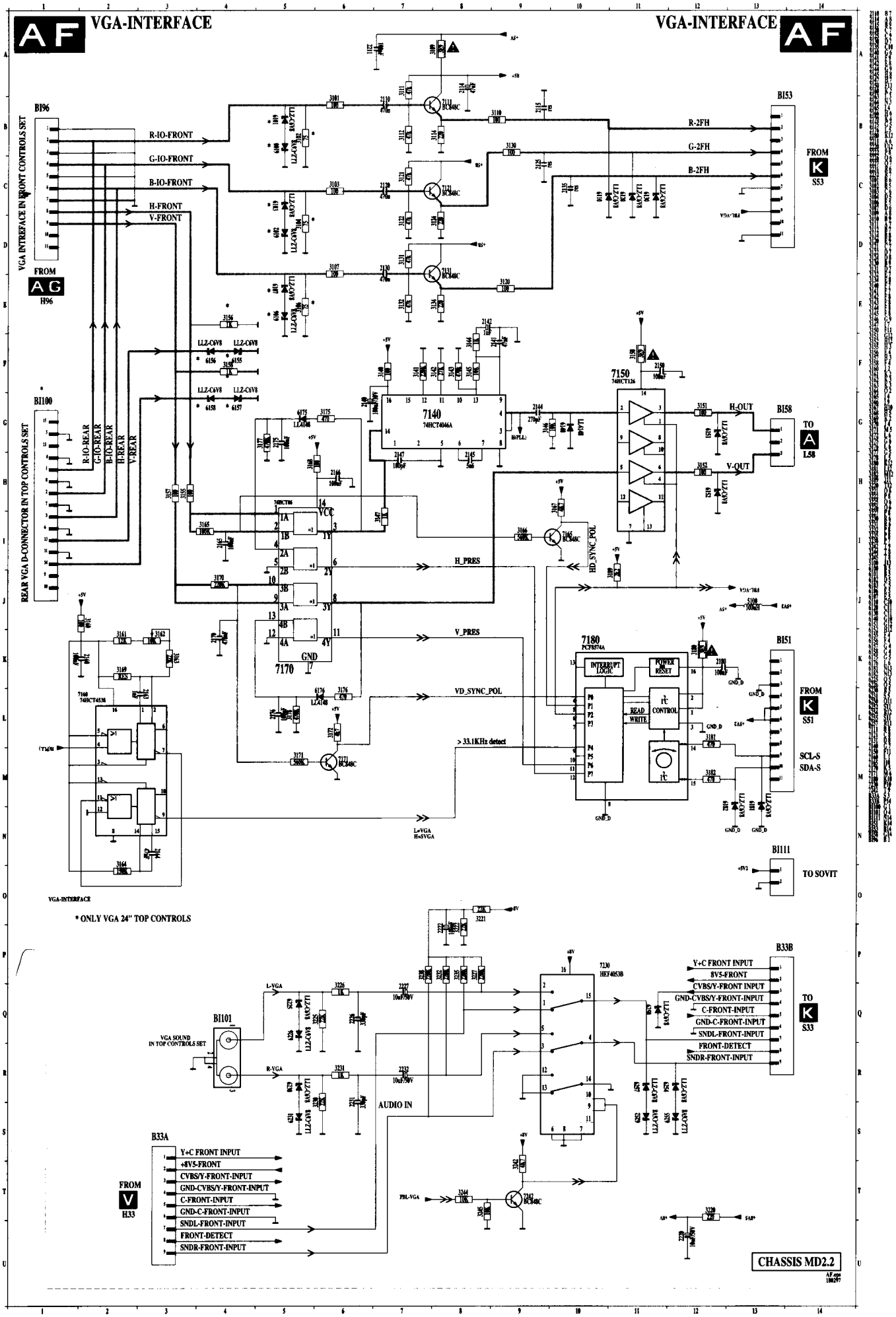
Schematic used for units 3104 217 04640
3104 217 04670
3104 217 05210
3104 217 05220

	3729	3730	3731	3741	3756	3757	
For unit 3104 217 04640 use	-	X	X	-	X	-	
3104 217 04670	-	X	X	-	-	X	
3104 217 05210	X	-	-	X	X	-	
3104 217 05220	X	-	-	X	-	X	

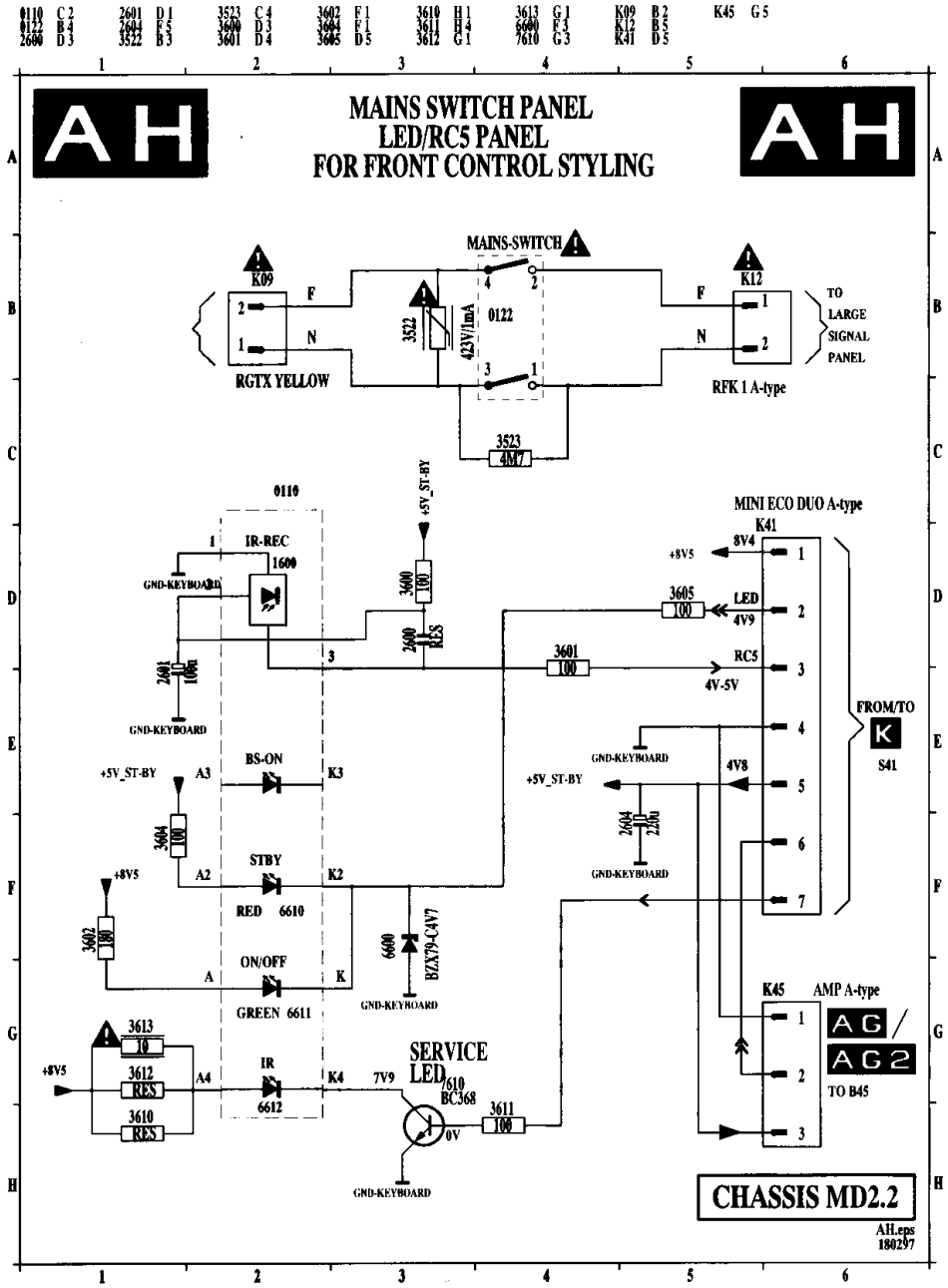
- = item not inserted X = Item inserted

(... V) MUTE STATE

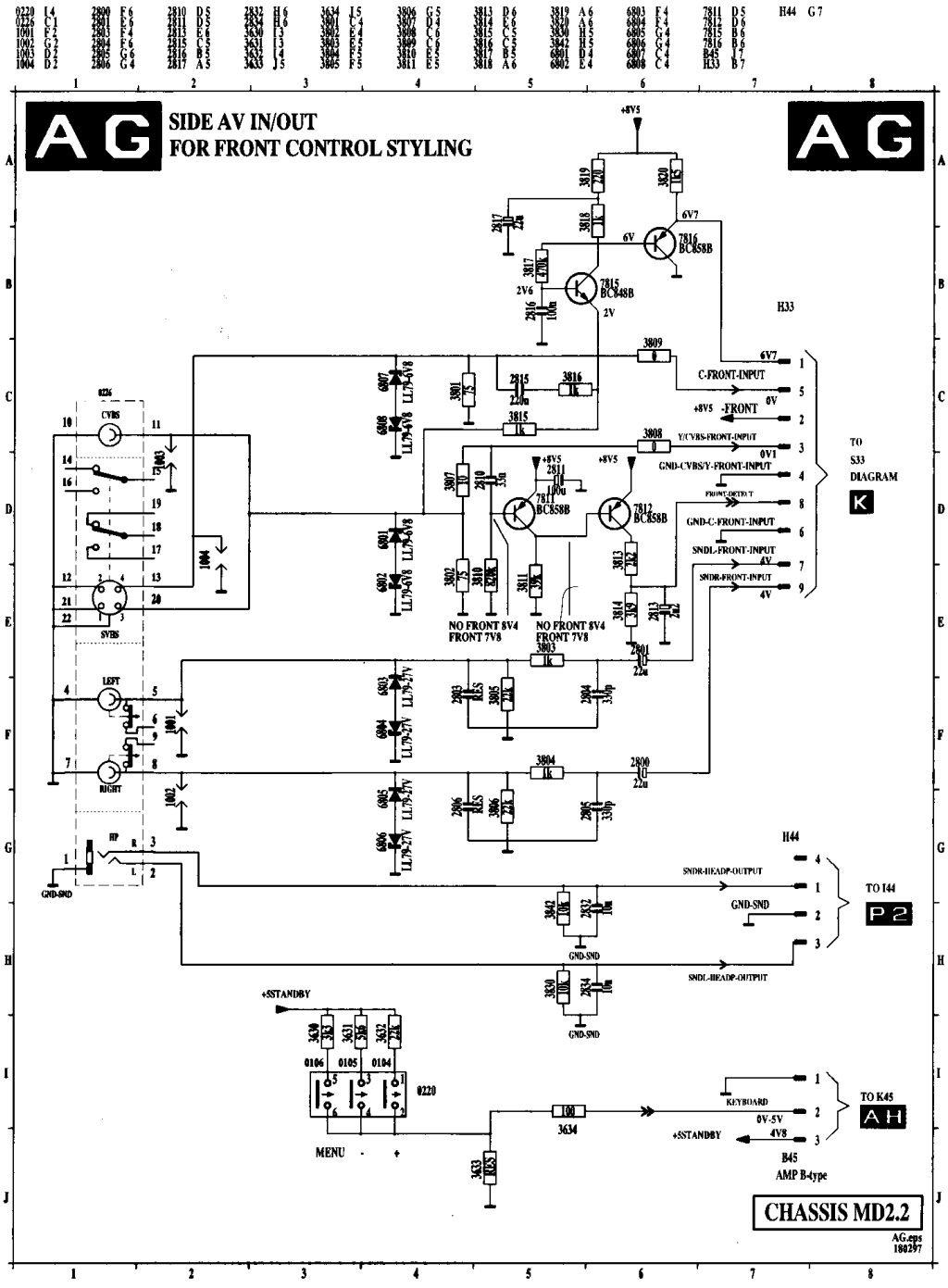
VGA interface panel / VGA-Schnittstellen-platine / Platine VGA-interface



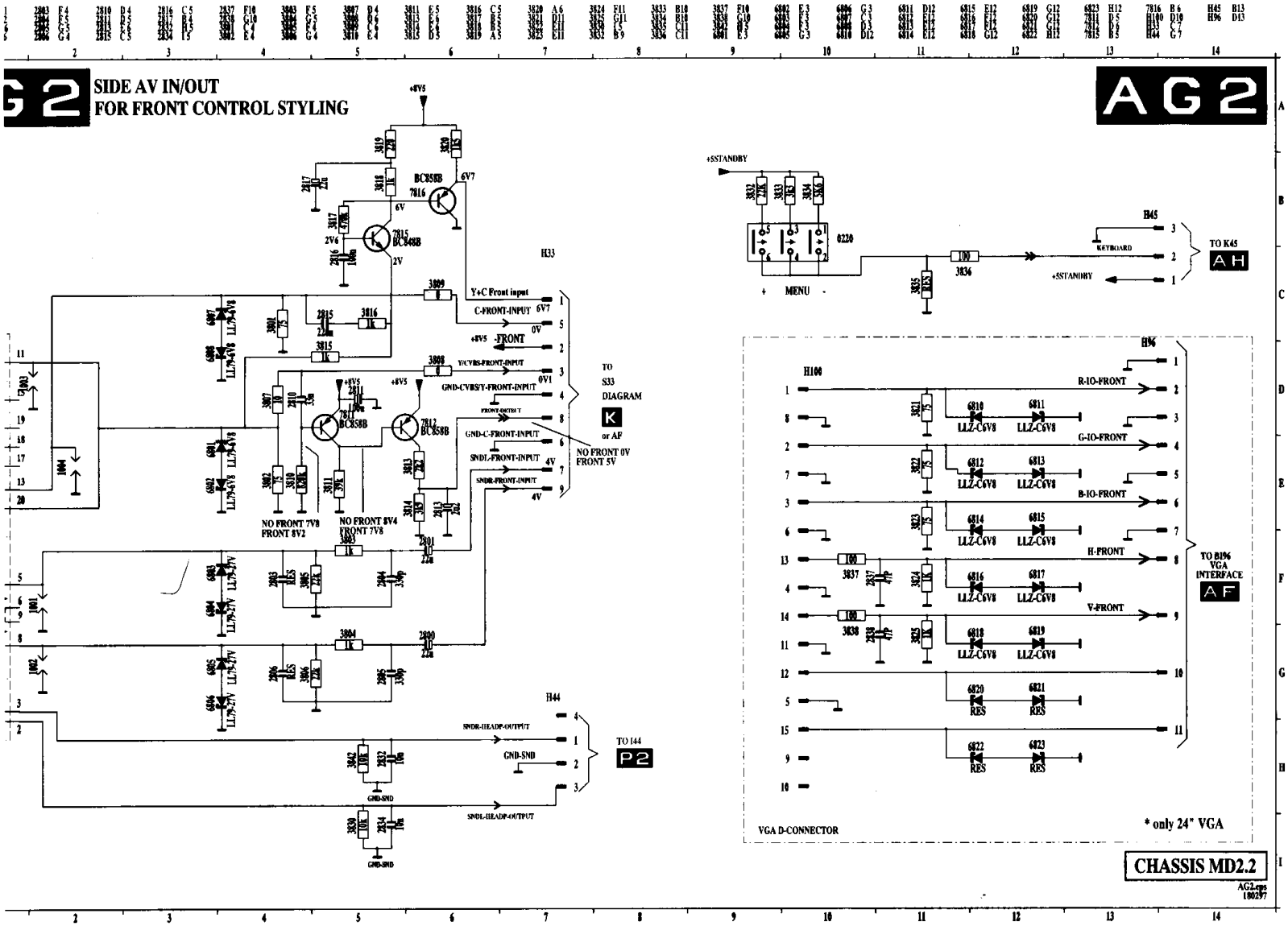
Mains input & RC5 panel (front control styling) / Netzeingang & RC5-Platine (Frontbedienung)/ Platine entrée secteur & RC5 (style commande de sur le haut)



Front input/output panel (top control styling) / Fronteingangs-/Ausgangsplatine / Platine frontale entrée/sortie



Front input/output panel with VGA input (front control styling) / Fronteingangs-/Ausgangsplatine mit VGA-Eingang / Platine frontale entrée/sortie avec entrée VGA



220 A 5	2804 A 1	2813 A 3	2834 A 1	3803 A 1	3808 A 4	3814 A 3	3819 A 3	3824 A 5	3834 A 5	3842 A 1	6804 A 1	6810 A 4	6815 A 4	6820 A 4	7812 A 2	H45 A 5
226 A 1	2805 A 2	2815 A 2	2837 A 4	3804 A 1	3809 A 3	3815 A 2	3820 A 3	3825 A 5	3835 A 5	3999 A 5	6805 A 1	6811 A 4	6816 A 5	6821 A 4	7815 A 3	H96 A 5
800 A 2	2806 A 2	2816 A 3	2838 A 4	3805 A 1	3810 A 2	3816 A 2	3821 A 5	3830 A 1	3836 A 5	6801 A 2	6806 A 1	6812 A 4	6817 A 5	6822 A 4	7816 A 4	H100 A 4
801 A 2	2810 A 2	2817 A 3	3801 A 2	3806 A 2	3811 A 2	3817 A 3	3822 A 4	3832 A 5	3837 A 4	6802 A 2	6807 A 2	6813 A 4	6818 A 5	6823 A 3	H33 A 3	
803 A 1	2811 A 2	2832 A 1	3802 A 3	3807 A 2	3813 A 3	3818 A 3	3823 A 4	3833 A 5	3838 A 4	6803 A 1	6808 A 2	6814 A 4	6819 A 5	7811 A 2	H44 A 1	